ELECOMP CAPSTONE SUMMIT
THURSDAY, MAY 7th, 2026

THE UNIVERSITY OF RHODE ISLAND

ENGINEERING SHOWCASE
FRIDAY, APRIL 24th, 2026

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OFDM-Sense

Simultaneous Communication and 2D Localization Leveraging OFDM Signals

ARCS LAB
ADVANCED RF/mmWAVE SENSING AND COMMUNICATIONS LAB

Team Members: O'Malley Sherlock (ELE), Royaljohn Southammavong (ELE)

Technical Director: Dr. Guoyi Xu

Project Motivation

Direction finding and localization of RF markers are critical technologies for next-generation telecommunication systems. With the rapid development of IoT devices in emerging domains such as autonomous vehicles and robotics, these networks require accurate environmental sensing at a scale order of magnitude higher than previously anticipated. However, bandwidth regulations and the need for power-efficient and compact hardware makes using separate communication and sensing systems undesirable.

To overcome these challenges, the industry is moving towards the integration of radar and communication functions into single, dual-purpose networks. This project aims to prototype this integration by leveraging orthogonal frequency-division multiplexing (OFDM). Because OFDM is the foundational modulation scheme in modern wireless standards, utilizing it allows us to develop a system capable of simultaneously transmitting data and location information within existing network architectures. This working system serves as a prototype for next-generation, dual-function communication networks with applications across urban, industrial, and transportation settings.

Anticipated Best Outcome

The ABO is to build a functional communication system prototype using software-defined radio (SDR) platforms operating within the millimeter-wave (mmWave) frequency range. The system must be able to transmit and receive OFDM packets on multiple channels in addition to performing RF localization. The ideal outcome would be a prototype for next-generation dual-function communication networks that may be used for IoT, robotics, and intelligent transportation functions.

- **ABO 1:** Understand working principles of OFDM communication through building a functional OFDM system using USRP X310 and Sivers EVK06002 modules
- **ABO 2:** Integrate pilot-based matched filter time delay estimation on a multi-channel communication system
- **ABO 3:** Simultaneous 2D localization and OFDM communication in a SIMO network

Key Accomplishments

SDR Platform Setup

The provided Software Defined Radio (SDR) hardware (USRP X310 and Sivers EVK06002 modules) were connected with RF cables and baluns. OFDM systems use the Inverse Fast Fourier Transform (IFFT) and Fast Fourier Transform (FFT) to encode and decode data symbols onto and from orthogonal subcarriers. To validate OFDM packet generation and transmission, single and multi-frequency sinusoidal waves with known frequencies were transmitted over direct wired connections. The single frequency sine wave test can verify if a specific subcarrier is correctly placed in the DFT domain, while the multiple frequency sine wave can verify if the subcarriers are truly orthogonal and non-interfering.

OFDM Transceiver Implementation

The core of this project involved developing a functional OFDM transceiver to run on the provided SDR hardware. The transmitter implementation included 16-QAM modulation, OFDM packet framing, and variable orientations of data symbols, pilot symbols, and synchronization symbols. The framed OFDM packet would be converted to a time-domain signal using an IFFT and sent over-the-air using the SDR hardware. The receiver end reverses the process by applying an FFT on the received signal. The received frequency domain data is recovered by correcting for channel distortions and frequency offsets before converting back into binary data. We achieved an average of <2% bit error rate (BER) in over-the-air transfers in a laboratory environment.

Packet Synchronization

The first step in recovering the transmitted data is to determine the index at which a packet begins in the received signal. This is known as synchronization and was implemented using the Schmidl-Cox synchronization algorithm. A known synchronization symbol is placed at the start of an OFDM packet. The Schmidl-Cox algorithm is a sliding-window algorithm that searches for the synchronization symbol and determines the start of the packet. Once the starting index is determined, it serves as a reference for the unpacking of subsequent symbols.

Carrier Frequency Offset (CFO) Correction

Small frequency differences between the transmitter and receiver's onboard oscillators shift the received signal's carrier frequency slightly. This frequency offset must be corrected to properly reconstruct the received OFDM data packet. CFO changes dynamically during transmission and must be calculated for every symbol. We implemented CFO correction by correlating the received packet's pilot symbol to the known transmitted pilot symbol across a frequency range to recover the original frequency. Data symbols have certain subcarriers allocated as pilot subcarriers (known by the receiver) and can be used to calculate the CFO for each data symbol.

Channel Estimation and Equalization

Wireless signals become distorted when traveling through non-ideal channels and media, i.e., air, reflections, absorptions, and interference all alter the amplitude and phase of each subcarrier differently. To correct this, the receiver uses the known pilot symbol in each OFDM data packet and compares it against the distorted received signal to calculate and apply channel gains for each subcarrier.

Zero-Padded Interpolation Matched Filter Delay Estimation

The sensing portion of the dual-function communication system was implemented by calculating the propagation delay between the transmission and reception of an OFDM packet. The matched filter cross-correlates the received signal with the known pilot symbol. Due to the speed of light and the hardware's low sampling rate, small changes in distance between the RX and TX will not cause a resolvable time shift in the raw sampled signal. Because the time delay is smaller than the sampling period, standard matched filtering yields only a coarse estimate. To achieve high-resolution delay estimation, frequency-domain zero-padded interpolation was implemented to artificially increase temporal resolution. The higher resolution allows for accurate delay estimation when delays are less than 1 sample in duration.

Multi-Channel Integration and Synchronization

Once single-channel OFDM communication was operational, the system was expanded to support multi-channel communication. This involved repeating the OFDM transfer and delay estimation algorithms across multiple receivers and one transmitter, including resolving any hardware synchronization issues.

2D Localization

A 2D multilateration localization algorithm was implemented to achieve the simultaneous communication and localization goal. The algorithm uses the Time Difference of Arrival (TDoA) of two RX devices to find the hyperbola of all possible values of the TX. After adding more RXs, the TX position can be estimated by converging on the intersection of the hyperbolas. To validate the localization system, Monte Carlo simulations were run alongside experiments with varying RX locations to recognize sources of bias and compare error margins.

Results

Average OFDM Evaluation Metrics:
Bit Error Rate: <1%
Symbol Error Rate: 3.2%
Error Vector Magnitude: 19.3dB

Localization:
Delay Variation: 0.043 ns
RMSE: 26.56 cm
P95 Error: 41.06 cm

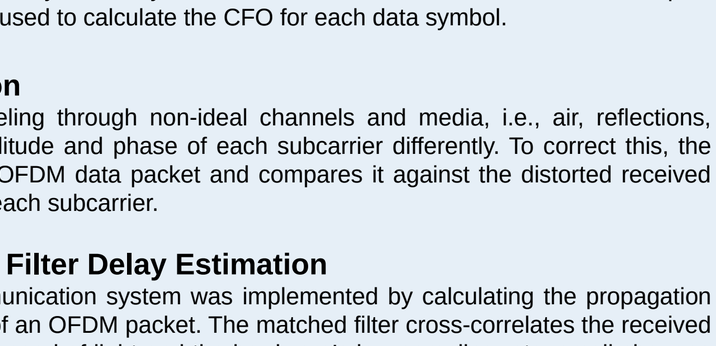

Figure 5. ~1.5 MB Over the Air Bitmap Image Transfer

Project Outcome

The project's anticipated best outcome was met. Our system is capable of simultaneous 2D localization and OFDM communication while also resolving carrier frequency offsets, channel estimation, and packet synchronization.

Figures

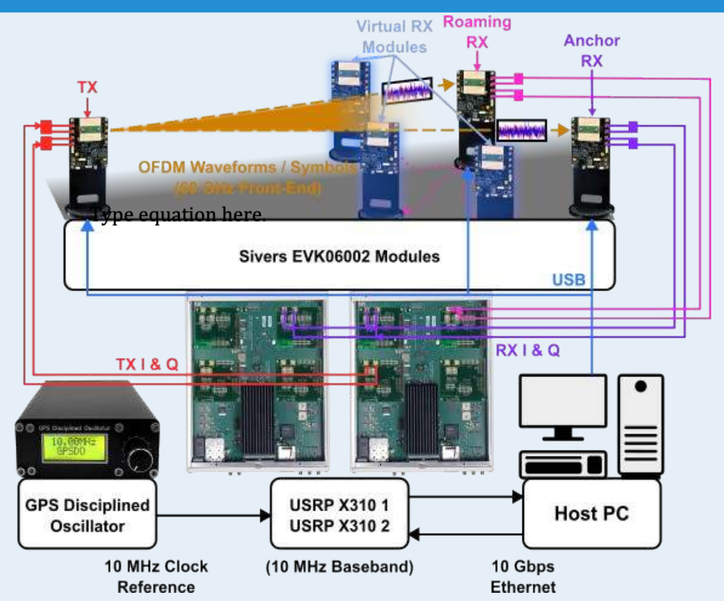

Figure 1. (a) Overall block diagram of system, (b) Experimental setup

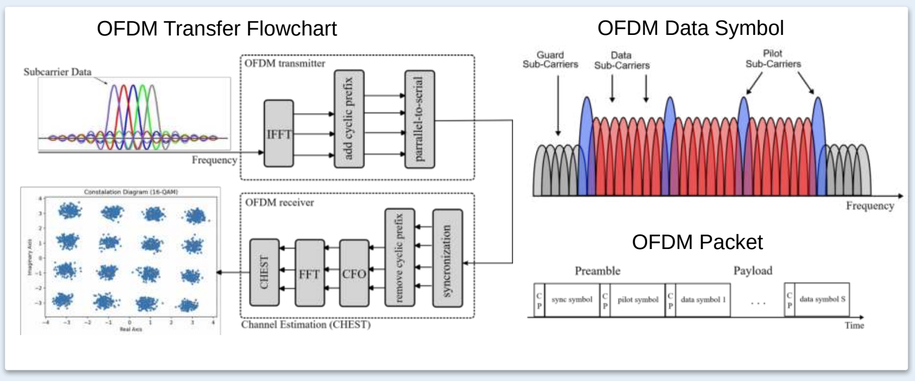

Figure 2. OFDM Transfer Flowchart, OFDM Packet and Symbol Structure

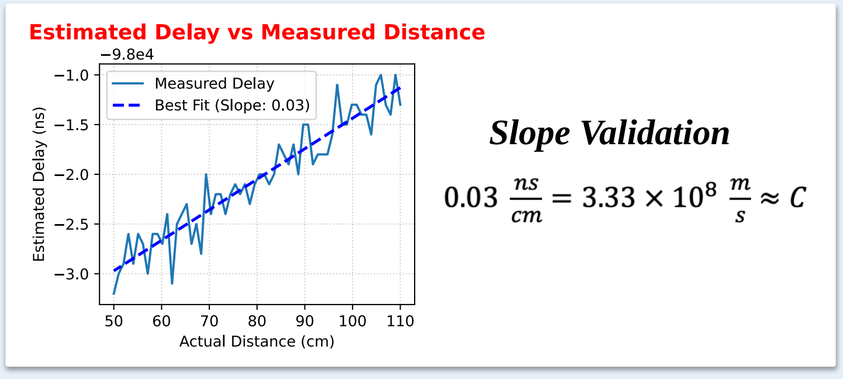

Figure 3. Zero-padded Matched Filter Delay Estimation Results

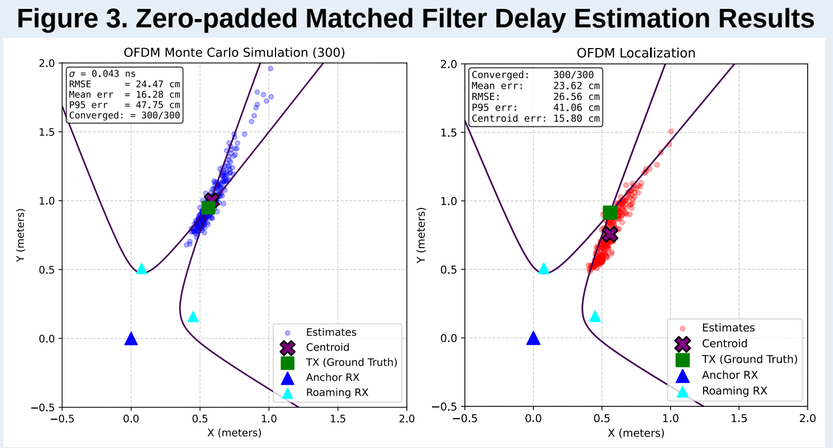

Figure 4. Localization Simulation (left) vs Measured Experiment (right)

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Real-Time Procedural Visual Aids

Boston Scientific
Advancing science for life™

Team Members: Jarrett DeFreitas(CPE), Noah Vargas (CPE)

Technical Director(s): Kevin Bagley, Dennis Hubbard, Prashanth Somu, Francesca Estey; CTD: Demetrios Petrou

Project Motivation

Endoluminal surgery is an emerging and rapidly evolving branch of advanced endoscopy, requiring clinical expertise, concentration, refined technical skill, and the use of highly specialized instruments to achieve safe and effective outcomes. As these procedures continue to occur, there is increasing interest in technologies that can support physicians during real-time decision-making. The integration of real-time visual aids represents an important proof of concept step toward demonstrating the feasibility of embedding machine learning based guidance into existing or future clinical systems. These visual tools are designed to enhance the workflow of endoscopists performing Endoluminal Surgery (ELS) by providing immediate information. The overarching motivation for developing such aids is to reduce the training time required for physicians to gain proficiency, lower cognitive load during demanding procedures, and decrease the likelihood of complications or operational errors. Ultimately, these advancements aim to elevate both safety and performance in endoluminal surgical practice.

Anticipated Best Outcome

The primary goal of the ELS Procedural Visual Aids Project is to develop proof of concept tools that demonstrate the feasibility of implementing real-time visual assistance during endoscopic procedures. Achieving this outcome will validate both the practicality and potential clinical value of integrating machine learning based visual aids into the workflow. In addition, the project aims to generate informed recommendations for future technological improvements, including enhancements in model performance, data processing, and system integration. These insights will guide the next steps toward producing and deploying a fully functional real-time assistance system.

Key Accomplishments

- **Dataset Creation**: A dataset was created in order to train the convolutional neural network. This was accomplished by taking open source videos of Endoscopic Submucosal Dissections(ESD) and splitting the video frame by frame.
- **Image Annotation:** The dataset comprising 6,000 images then had to be annotated using image segmentation. With the tool CVAT 1000 instances of blood vessels have been annotated so they can be used in the training of an accurate model. Image segmentation is the process of partitioning particular images into different sections so they can be used in a meaningful analysis.
- **Model Selection:** The convolutional neural network that is most apt for real-time image processing is a You Only Look Once(YOLO) model. YOLO models operate by dividing an image into a grid and predicting bounding boxes, classes, and segmentation masks in a single forward pass through the network making them significantly faster than other CNN models. **(Fig. 1)**
- **Dataset Interpretation:** To maximize the value of the dataset created, transformations of annotated frames were implemented. This means by rotating, flipping, and changing the hue of each blood vessel annotated we can increase size of the dataset multiplicatively.
- **Model Training:** Training was done using the UNITY cluster provided by the University of Rhode Island that houses GPUs that are able to handle the dataset. The number of training epochs was increased while implementing measures to prevent overfitting, ultimately producing a model with 70% precision and recalling 63% of all blood vessels. **(Fig. 2)**
- **Model Visual Inference:** To visualize the model's predictive capabilities, video inference was implemented on pre-recorded endoscopic footage. This was accomplished using the Ultralytics predict method, allowing the model's detections to be observed and evaluated across full video sequences.
- **Real-Time Inference Using Screen Recording:** The model was adapted to perform inference on live screen recordings, enabling real-time predictions to be generated and visualized directly from captured screen output rather than pre-recorded video files.
- **Elgato Video Capture:** To obtain a live video feed suitable for real-time model inference, an Elgato 4K capture card was integrated alongside Elgato Studio software. This setup enabled the model to process and analyze live endoscopic video as it was being captured.
- **Real-World Deployment Testing:** The Elgato video capture and real-time inference pipeline was deployed and tested in an active lab setting. This evaluation verified the system's ability to function outside of a controlled development environment and provided insight into practical performance considerations.
- **Automatic Power Switch Prototype:** A first iteration of an automatic power switch was developed, driven by the computer vision model to dynamically control the wattage of an electrical surgical knife. This prototype demonstrates the potential for the system to directly interface with surgical equipment based on real-time model predictions.
- **Real-Time Inference Streamlining:** The real-time inference program was refined and optimized to improve usability and functionality. Enhancements included the addition of window selection capabilities and the ability to save outputs in multiple formats, including a CSV file and a recorded video of the inference session. **(Fig 4)**
- **Executable Creation:** To improve accessibility and ease of deployment, the real-time inference program was packaged into a standalone executable. This allows the system to be run without requiring a development environment, lowering the barrier for use in clinical or lab settings.

Project Outcome

The project has successfully achieved its Anticipated Best Outcomes. The team has demonstrated the feasibility of real-time visual assistance during endoscopic procedures, validating the potential clinical value of machine learning-based visual aids. The team has also provided hardware recommendations, and possible technology modifications/enhancements to Boston Scientific.

Figures

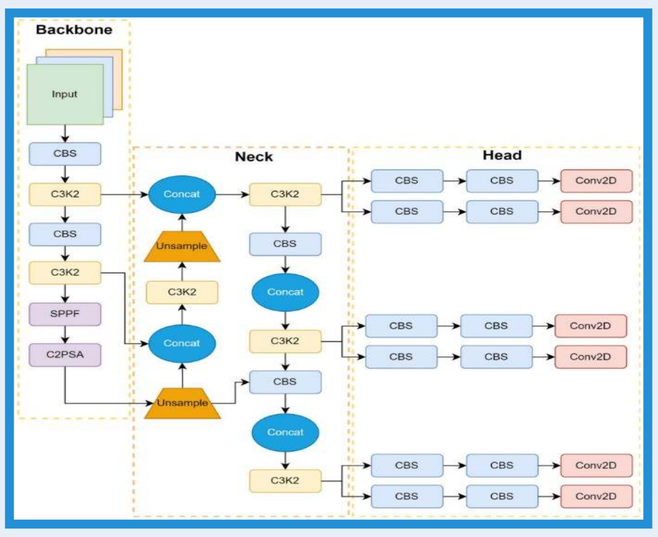

Figure 1: Architecture of YOLO-v11

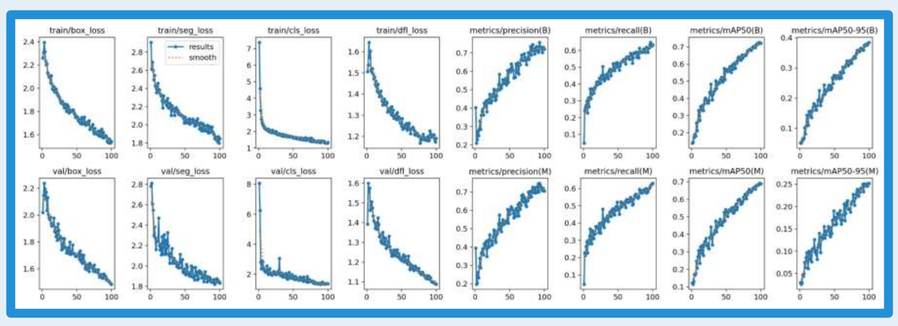

Figure 2: Model Metrics

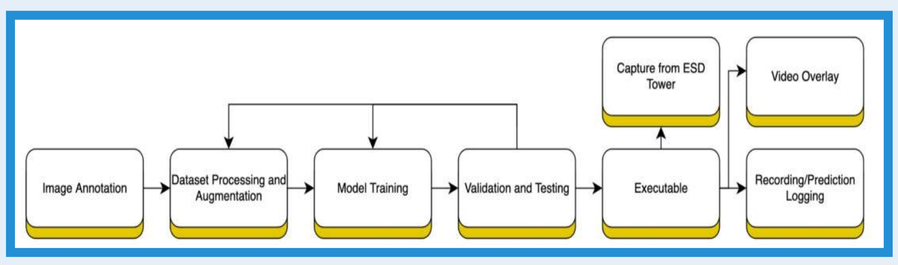

Figure 3: Project Block Diagram

Figure 4: Real-Time Inference Example

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Brain Stimulator

Transcranial Pulsed Current Stimulator (tPCS)

Team Members: Jarad DeMarco - Electrical Engineer

Technical Directors: Mike Smith

Project Motivation

- Combining electronics and medical technology
- Interest in how the brain functions
- To understand the connection between embedded software, hardware, digital and analog technology
- Interest in a cure for depression and movement disorders

Anticipated Best Outcome

- Device produces even biphasic pulsed current
- User selects charge / system selects current
- LCD shows updated real current
- The GUI is easy to use
- Systen is a closed loop measurement system
- Device enforces state machine safety transitions
- Device maintains stable current over normal skull impedence

Key Accomplishments

- Scrapping the four other VCCS designs I was using then finding and choosing a new design that improved accuracy by more than 99 %.

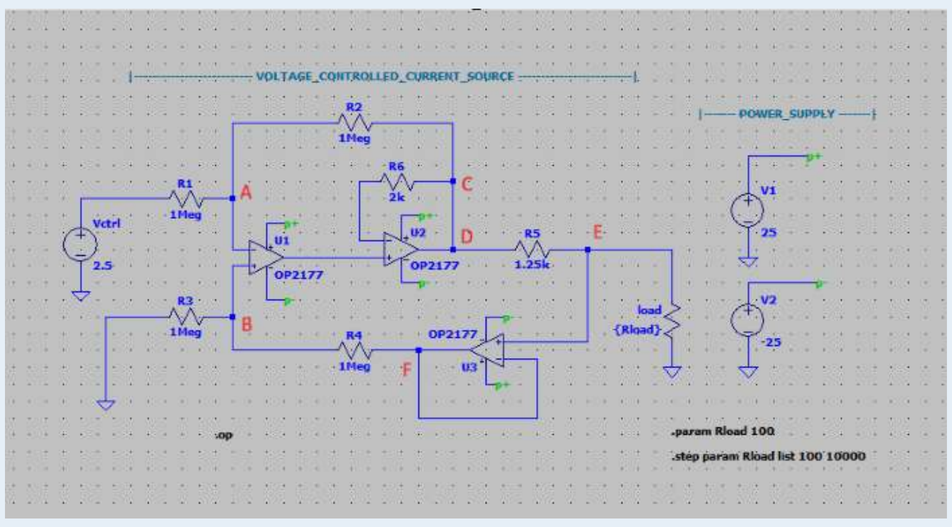

Fig 4: New and Improved Howland Style Voltage Controlled Current Source (VCCS)

- Designing a level Shifter that I realized would invert one of the channels after solving its transfer function

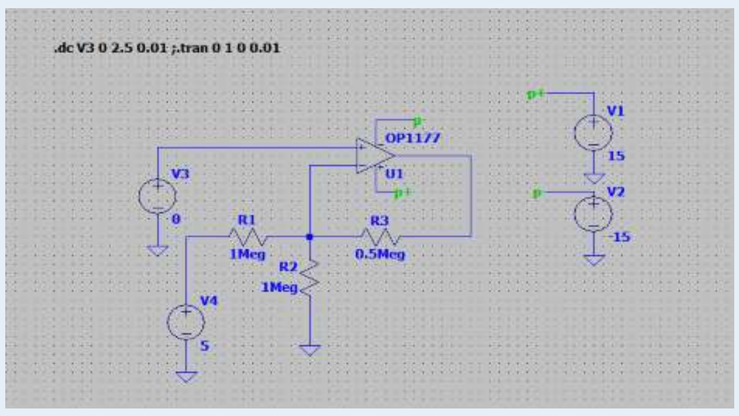

Fig 5: Level Shifter

- Successfully soldering very small connections on the chips
- Build the firmware to convert digital values to voltages using a DAC with I2C
- Designed an intuitive four button user interface
- Found the simulation version of the models I would be purchasing and simulated them before the real device was built so I could troubleshoot all problems in simulation.
- Tested the device with a potentiometer ranging for zero to 10 k Ohms to verify performance
- Implemented hardware timer interrupts for better timing control
- Built the GUI so that it gives user instructions and shows user the actual output current
- Developed the code with a state machine style for better safety
- I learned about the different uses of brain stimulators and chose mine because the current amplitudes and phase width are the values that treat depression
- I learned about the things that would need to change if this were to be a real medical device
- I correctly soldered the chips to the breakout boards
- I learned how to use Digikey, go through its filters and create a parts list
- I implemented a device that uses embedded code, hardware, digital and analog technology
- The system is based on the user selecting charge instead of current because that is the important value that must inverse after every pulse width
- I combined electronics and medical technology

Project Outcome

On the first plug we obseverved the brain stimulator worked exactly as it should on the oscilloscope as you can see in figure 1. All anticipated best outcomes were met.

Figures

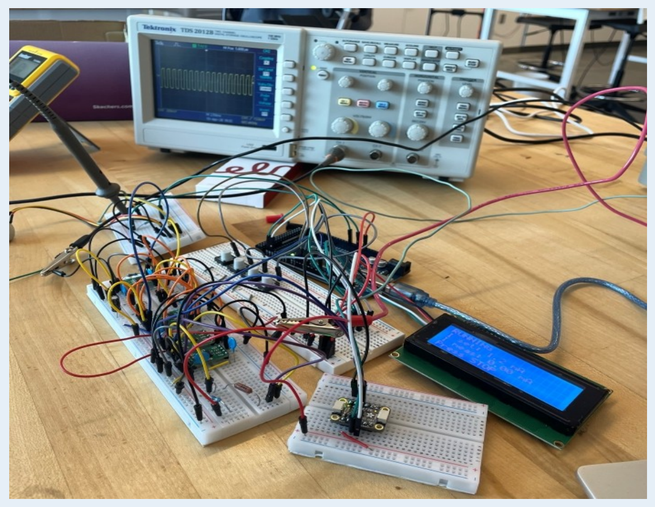

Fig 1: Final Test

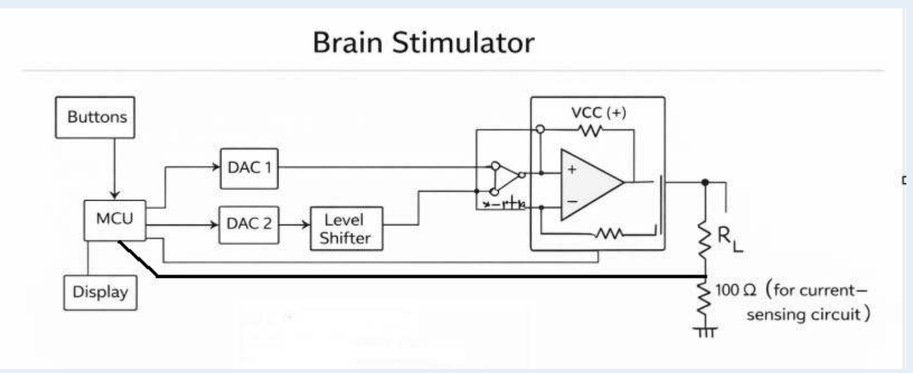

Fig 2: Top Level View

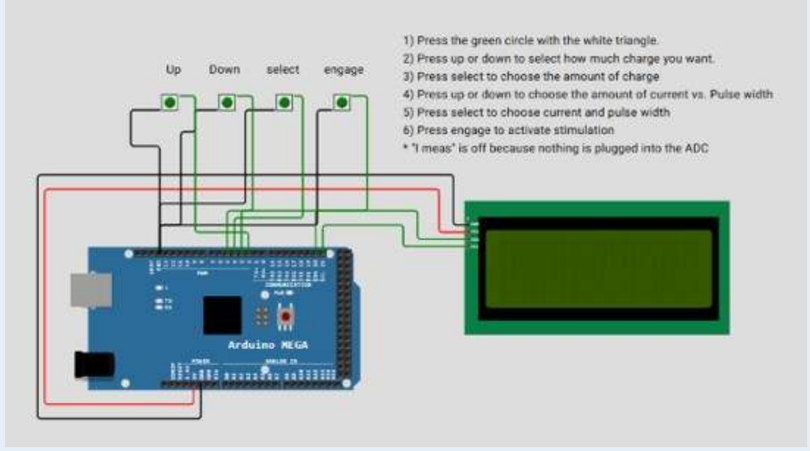

Fig 3: GUI

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Digitrap

An intelligent lobster trap

Team Members: Kevin Vu (CPE), Jacob Phillips (ELE), Anna Civitillo (ELE)

Technical Director(s): Colin Vincent, Connor Vincent, Zach Lindo, & Hayden Radke; CTD: Mike Smith

Project Motivation

The functionality of underwater traps intended for harvesting marine species is questionable. Additionally, the ropes tied to conventional underwater traps can get caught and harm other aquatic life not meant for harvesting. DBV Technology has created a new, ropeless lobster trap meant for safer and sustainable harvesting, but monitoring the success of the trap falls into the same pitfalls as conventional traps: there is not much available to monitor the success of the trap while it is deployed. In our capstone project, we will design and test a system that can collect data in underwater traps, specifically a lobster trap, to both monitor the success of DBV Technology's new trap as well as provide research data on marine animal behavior and oceanographic conditions. This project will integrate sensors, cameras, and embedded computing to create a reliable data collection platform.

Anticipated Best Outcome

The students will design, build, test and demonstrate an intelligent lobster trap – DigiTrap that will meet a set of requirements provided to them. The design activities will encompass market research, electrical hardware design, software design, and mechanical packaging design.

Key Accomplishments

Designed schematics made up of four different sections titled MCU_Full, MCU_Power, RaspberryPi, and Power with a larger Top_View file connecting the different subsystems together. MCU_Full contains the STM32U535RBT6 Microprocessor, sensors connected to it, and additional relevant components like the user button and SD card reader. MCU_Power contains power nets and capacitors necessary to provide smooth and stable power to the microcontroller. RaspberryPi contains the 2x20 pin connector which will plug directly into all GPIO pins in the Raspberry Pi 5 Computer, providing the Pi with power and communication channels with the microcontroller. Lastly, the Power section contains converters that step the battery voltage from the battery pack's 36V down to 12V for lights, 5V for the computer, and 3V3 for the microprocessor. This section also contains load switches for the lights and computer, as well as an optional 5V LC filter to reduce noise. These designs were laid out on a 2.2 x 4.5inch PCB designed to stack directly on top of the Raspberry Pi 5 computer.

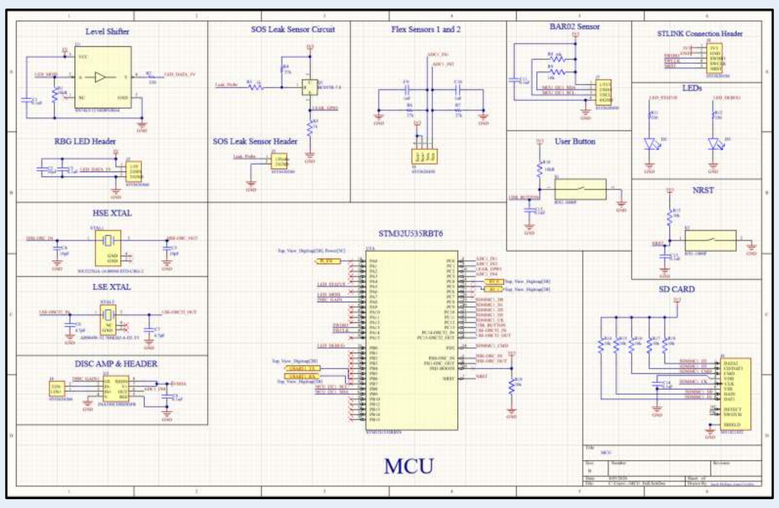

Figure 4: MCU Schematic

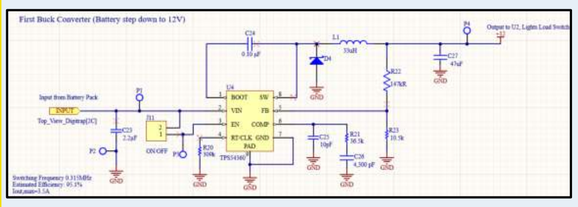

Figure 5: 36V to 12V Buck Converter in Power Schematic

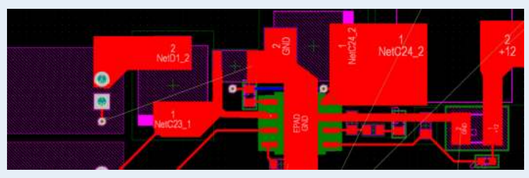

Figure 6: 36V to 12V Buck Converter in Layout

Designed and implemented a low-power embedded system integrating an STM32U5 microcontroller with a Raspberry Pi 5 to support real-time environmental monitoring and event based data collection (Figure 3). Successfully interfaced multiple sensors using I²C and UART protocols, including development of custom STM32 HAL drivers adapted from existing Arduino libraries. Established reliable intercommunication and validated system performance through hardware testing, enabling accurate sensing, data processing, and controlled activation of higher-power subsystems.

A robust data pipeline was established between the STM32U5 microcontroller and Raspberry Pi 5, enabling seamless UART-based communication for real-time sensor data transmission and command handling. A live demo was successfully developed using the STM32 Nucleo board, where a button press triggers the Pi to begin camera recording, validating the full end-to-end hardware and software integration. Firmware was implemented on the STM32U5 to manage sensor acquisition, packet formatting, and protocol handshaking, while corresponding Python code on the Pi handles serial communication, camera control via picamera2, and session recording, forming the complete software foundation of the DigiTrap system.

Project Outcome

The project successfully achieved full PCB development and complete firmware implementation, establishing a functional embedded system architecture. While comprehensive system-level beta testing was not completed within the project timeline, the design and integration efforts position the system for immediate validation and deployment in future work.

Figures

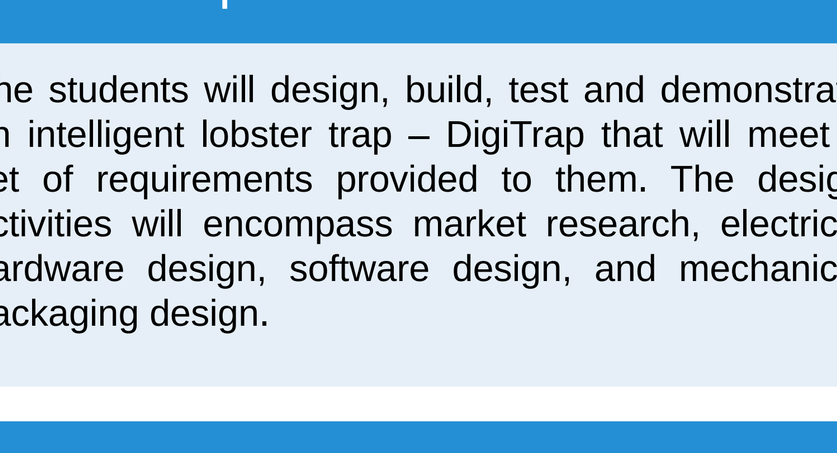

Figure 1: Workflow Diagram of Recording to File Transfer

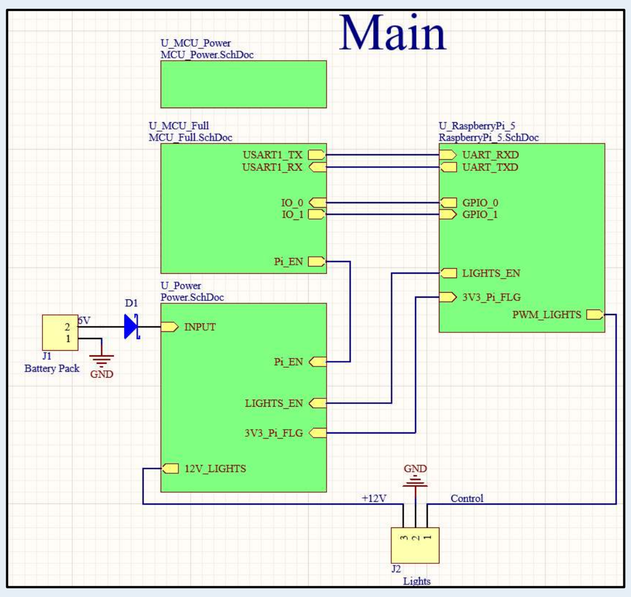

Figure 2: Top Level Schematic

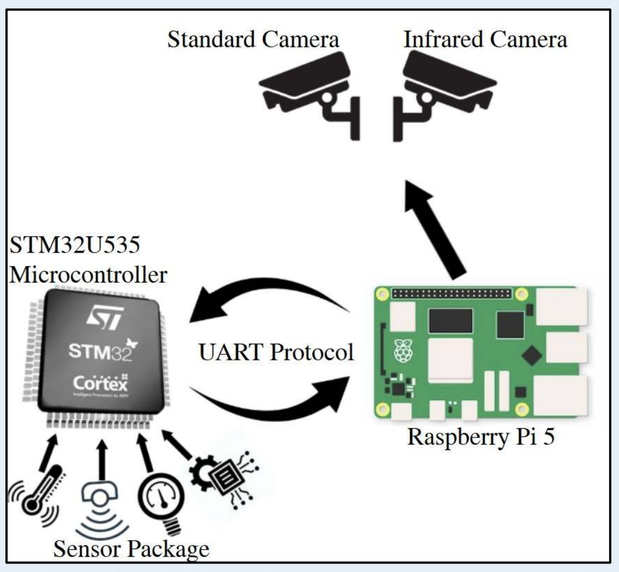

Figure 3: High level intercommunication graphic

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Edge Computing on GPUs for Ground Robotics

DRAPER®

Team Members: Sarah Eisenstein (CPE), Ben Gulezian (ELE), Mckenna Sylvester (ELE)

Technical Director(s): Stephen Lawrence, Rick Wang, & Mike Smith (CTD)

Project Motivation

The project is motivated by Draper's long-standing leadership in autonomy, edge computing, and multi-agent systems. Draper develops algorithms and software that support autonomous missions across underwater, terrestrial, aerial, and space environments, and the need for compact, intelligent, collaborative robotic platforms continues to grow. This project aims to enable a swarm of small ground robots to explore and map cluttered indoor spaces using onboard computation and centralized coordination. By building an edge-compute infrastructure that fuses local sensing with shared mapping, the team advances Draper's goal of demonstrating scalable swarm autonomy. The motivation also reflects broader challenges in robotics, especially operating reliably in GPS-denied, visually cluttered office environments. Creating robots that can interpret their surroundings, share information, and maintain situational awareness is essential for future autonomy architectures. This work lays the foundation for systems that are efficient, resilient, and deployable across diverse operational

Anticipated Best Outcome

The anticipated best outcome is a functional prototype demonstrating edge computing for swarm autonomy across multiple ground robots. At the baseline level, the system will perform 2D SLAM, centralized map fusion, and visual marker detection. Advanced outcomes include coordinated navigation between at least two robots using shared logic. Stretch goals expand into 3D mapping through stereo or monocular cameras and CUDA-accelerated perception tasks. Collectively, this prototype will validate Draper's ability to deploy collaborative indoor exploration systems that combine onboard processing with centralized intelligence, ultimately showcasing a scalable model for future autonomy platforms.

Key Accomplishments

JetBots: Successfully built and wired three ground robots, achieving fully functional headless operation (no monitor required) (see Fig. 4) Enabled secure and efficient control through SSH for streamlined deployment.

ROS2 Workspace Development:

Motor Node: Verified successful workspace builds and ensured compatibility with ROS2 nodes running on Jetson systems.

Raft Stereo Camera Node: Developed a GPU-accelerated stereo vision node to provide real-time visual feedback, enabling depth estimation and perception (see Fig. 3).

IMU Integration: Incorporated IMU data for improved localization and motion tracking.

System Integration: Compiled and deployed all nodes onto the Jetson platform, enabling cohesive operation and supporting 2D SLAM functionality.

GPU Acceleration:

Transitioned key processing tasks from CPU to GPU, significantly improving performance in depth estimation and real-time mapping (see Fig. 3).

2D SLAM Implementation:

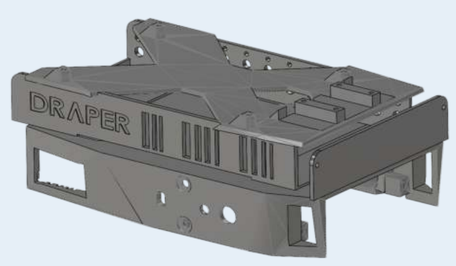
- Achieved real-time localization using stereo camera depth data.
- Generated continuous position estimates for navigation in dynamic environments.

Point Cloud 3D Mapping:

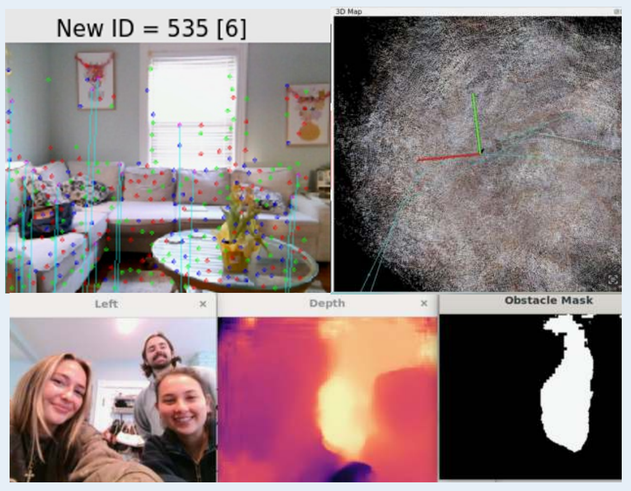
- Captured full XYZ spatial data for environmental reconstruction.
- Visualized robot trajectory using a teal path to indicate movement history.
- Projected visual feature points (key points) from camera images ee Fig. 3).

Figures

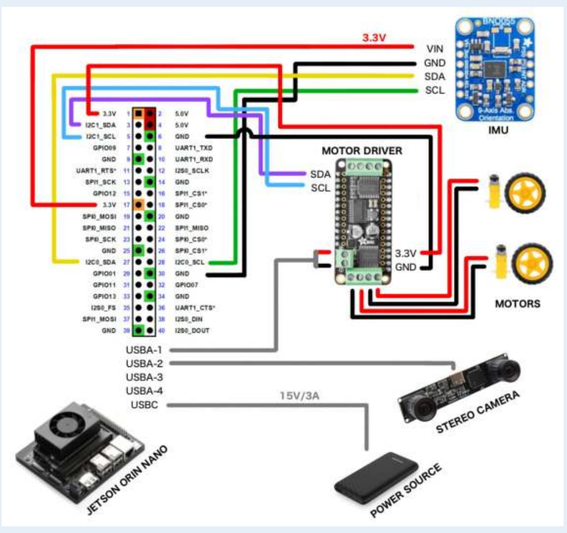
The JetBot swarm depicted in scanning a complex environment (Fig. 1)



The chassis model for the JetBot (Fig. 2)



Live stereo camera depth, obstacle mask, and point cloud 3D mapping generation from the JetBot (Fig. 3)



JetBot wiring diagram (Fig. 4)

Project Outcome

A multi-robot edge-computing autonomy system designed for mapping and navigation. The system consists of three compact ground robots, each built on a Jetson-based embedded GPU platform, enabling onboard processing and real-time decision-making without reliance on external computation.

These components are interfaced through a custom wiring architecture that supports reliable power distribution and signal communication. The robots are designed to operate headlessly, with secure shell (SSH) access enabling remote control, monitoring, and code deployment without requiring a physical display.

The system is built within a ROS2 framework. Each robot runs a collection of nodes responsible for motor control, sensor data acquisition, camera streaming, and odometry calculation. These nodes communicate through ROS2 topics, allowing modular and scalable functionality. The robots are capable of performing 2D SLAM (Simultaneous Localization and Mapping), generating maps of their environment while tracking their position within it.

A key feature of the system is inter-robot communication over a shared local network. Robots exchange relevant data such as positional information and mapping updates, enabling coordinated operation and contributing to a unified mapping objective. GPU acceleration is utilized to enhance computational performance, particularly in depth estimation and mapping tasks, resulting in faster and more efficient processing compared to CPU-based implementations.

The system is designed for flexibility, allowing easy updates through a shared GitHub repository and enabling further development or scaling.

The prototype demonstrates a cohesive integration of hardware and software, delivering a scalable and efficient platform for autonomous multi-robot exploration using edge computing.

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Safety Critical Applications for RISC-V Platforms

DRAPER®

Team Members: Jaime Iglesias (CPE) and Shane Stamp (ELE)

Technical Director(s): Steve Lawrence, Mike Smith, Jeshua Benzant, and Jesse Sullivan CTD: Mike Smit

Project Motivation

Safety-critical embedded systems need to be predictable, secure, and easy to verify. Our project focuses on using an open-architecture RISC-V platform combined with Rust to explore how memory-safe software and transparent hardware can improve reliability in real-time applications. Rust removes many of the common issues found in traditional embedded languages, while RISC-V provides full visibility into the hardware without relying on closed toolchains or proprietary features. To test these ideas, we are using the mechanical “Shoot-the-Moon” game as a real-world environment that requires accurate sensing, fast reaction times, and precise servo control. The game provides a simple but technically demanding system where timing, driver design, and hardware behavior directly affect performance. The motivation for the project is to understand how memory-safe software and open hardware behave together in a real-time, sensor-driven application.

Key Accomplishments

- **System Architecture Design**
  Developed a complete hardware-software architecture integrating the VisionFive 2 RISC-V platform, LiDAR sensor, and servo actuator. The system was structured into sensing, control, and actuation layers to improve modularity and scalability. (**See Fig. 1**)
- **Rust-Based Embedded Implementation**
  Implemented core system functionality in Rust to leverage memory safety and concurrency guarantees. This approach minimizes risks such as memory leaks and undefined behavior common in traditional embedded systems.
- **LiDAR Sensor Integration**
  Successfully interfaced the LiDAR sensor with the RISC-V platform using a custom driver implemented through Rust and C interoperability. Real-time sensor data is used to determine system state and ball position. (**See Fig. 2**)
- **Servo Control System**
  Developed a servo control mechanism using PWM signals to achieve precise angular positioning. Bench testing confirmed accurate and stable signal generation.
- **Control Algorithm Development**
  Implemented a feedback-based control algorithm to dynamically adjust platform position based on sensor input. The system minimizes overshoot and improves response time during operation.
- **Hardware Integration and Assembly**
  Constructed the full system including electrical wiring, breadboard connections, and mechanical mounting. Iterative testing ensured reliable connections and system functionality. (**See Fig. 3**)
- **QEMU Development Environment**
  Established a RISC-V emulation environment using QEMU to support early-stage software development and debugging prior to full hardware integration.
- **Signal Validation and Testing**
  Verified PWM signals and control outputs using signal generators and measurement tools to ensure correct timing and electrical performance.
- **System Tuning and Optimization**
  Performed iterative tuning of control parameters, including gain adjustments and sensor thresholds, to improve system stability and accuracy.
- **Mechanical Design and Fabrication**
  Designed and fabricated custom 3D-printed mounts for the LiDAR sensor and structural components. This improved alignment and overall system robustness. (**See Fig. 4**)

Anticipated Best Outcome

The anticipated best outcome is a fully functioning physical system, running on a RISC-V platform, that can reliably play Shoot-the-Moon with at least 80% accuracy from a fixed initial state. This includes robust drivers interfacing with Rust, a clean dependency-injected control architecture, stable and repeatable sensor measurements, and smooth, predictable servo actuation. In parallel, we will provide a QEMU-based RISC-V environment capable of booting the StarFive OS image so early development and testing can occur without immediate access to the hardware.

Project Outcome

The project successfully achieved the anticipated best outcome by implementing a RISC-V based control system that integrates LiDAR sensing and servo actuation to reliably control the ball position. The system met core performance goals, demonstrating consistent operation from a fixed starting position.

Figures

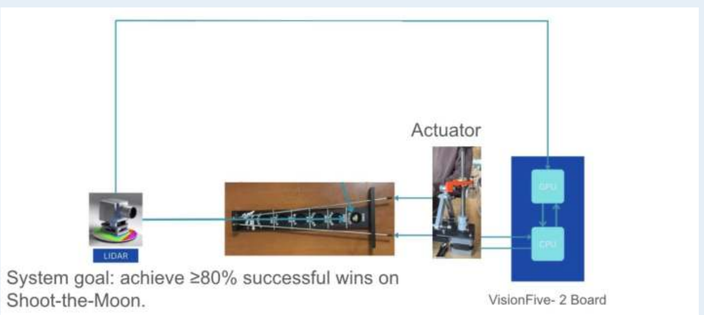


Fig. 1 – System Architecture Diagram

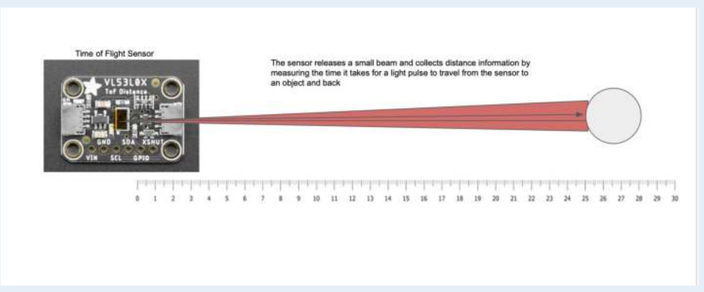


Fig. 2 – LiDAR Sensor Integration

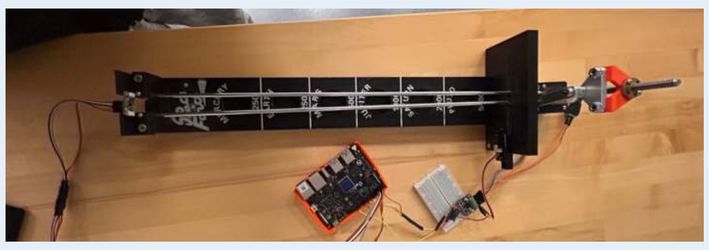
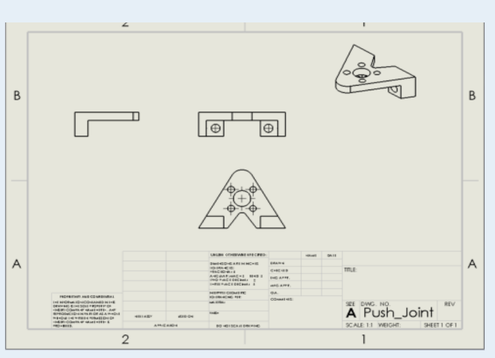


Fig. 3 – Full Hardware Setup



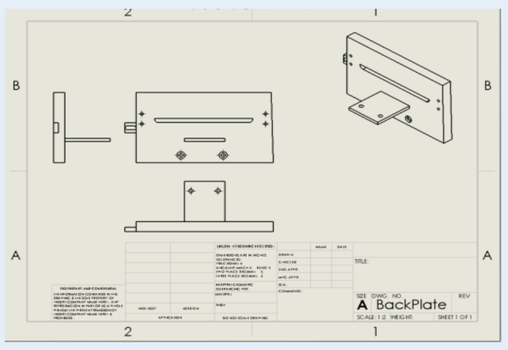


Fig. 4 – Mechanical Design Components

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ElectroStim

Electrical Stimulator for Muscular and Neural Biomedical Research Applications

Team Members: Thomas Vrankar (ELE CPE)

Technical Director(s): Dhaval Solanki, PhD

Project Motivation

This project strives to develop a portable and low cost electrical stimulation system for biomedical applications such as pain management, rehabilitation, and neurophysiology research. The design integrates programmable stimulation circuitry, a microcontroller-based control unit, and a user-friendly interface with potential biosensing feedback. The overall concept of this project is to create a system that works as a multi-channel electrical stimulation platform, designed to deliver controlled electrical pulses to biological tissue for therapeutic or research applications. This device can be applied to deliver either brain or muscle stimulation, depending on the needs of the patient. The project motivation focuses on developing a compact, cost-effective, and customizable multi-channel electrical stimulation system for biomedical applications. Electrical stimulation is often used to treat conditions like pain, muscle atrophy, and neurological disorders, however current systems are often bulky and expensive. The project aims to create a programmable device that supports personalized and wearable therapies, combining engineering principles with real-world healthcare needs.

Key Accomplishments

Schematic: The circuit design consists of 4 important sections - rail voltage regulation, high voltage control, feedback, and user interfacing

- Rail voltage regulation scales the 12V battery pack input voltage for powering the many ICs and microcontrollers. The 12V is given to two positive linear regulators, generating 5V and 3.3V respectively. The 5V is provided to the positive rail of feedback op amps, as well as powering the peripheral microcontroller. The 12V is also provided to an inverting charge pump and -5V linear regulator, providing the negative rail voltages for any op amps which are not rail-to-rail.

- The high voltage controller is responsible for varying the output voltage of the device proportionate to the voltage emitted by the peripheral DAC. The DAC can emit any voltage between 0 and 3.3V with 1024 steps of precision. This voltage is provided to a high voltage Op Amp with 50V on the positive rail and a gain of 15, Multiplying the 3.3V maximum output to 50V. This output voltage is then given to a series of integrated half-bridges, controlled by digital outputs from the MCU.

- The feedback portion of the circuit is intended to measure momentary voltage and current. Voltage sensing is accomplished via a voltage divider which scales the output to be between 0 and 3.3V to give to the ADC. The current sensing drops a voltage across a known shunt resistance, uses a differential amplifier to output the voltage drop, multiplying the value to be between 0 and 3.3V, again for the MCU ADC. Since the current will be in the form of a square wave with 5ms peaks, the current sensor also includes a peak detector circuit to output the highest current present.

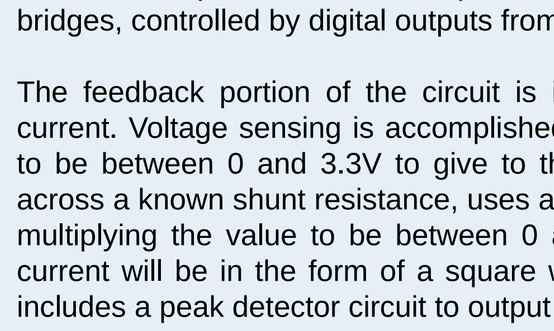
- The user interfacing circuitry includes buttons for control and various indicator LEDs.

Board Layout: The PCB designed in this project is a 2-layer board with separate analog and digital grounds and designed to minimize additional noise. Decoupling capacitors are included close to the pins of ICs as possible. Its modular design allows for easy connection of multiple channels in the future, allowing up to 8 total without exceeding available power.

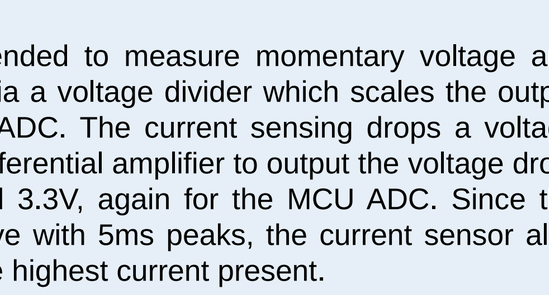
Software: The embedded firmware is the core of the closed loop control system. The central MCU (Arduino Due) is responsible for reception and processing of user inputs, and for relaying thise interpreted inputs to the peripheral MCU via I2C protocol, which is responsible for voltage regulation and current/voltage sensing. Based on measured voltage and current values compared to desired values, the DAC output is altered according to a simple search algorithm used to determine the correct output setting without ever exceeding safe current levels

Results:

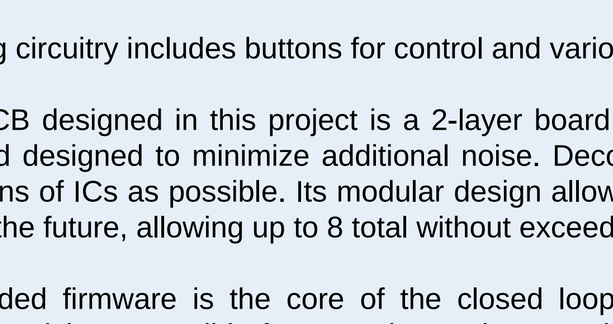
Infrequent Mode



Frequent Mode



Constant Stimulation Mode



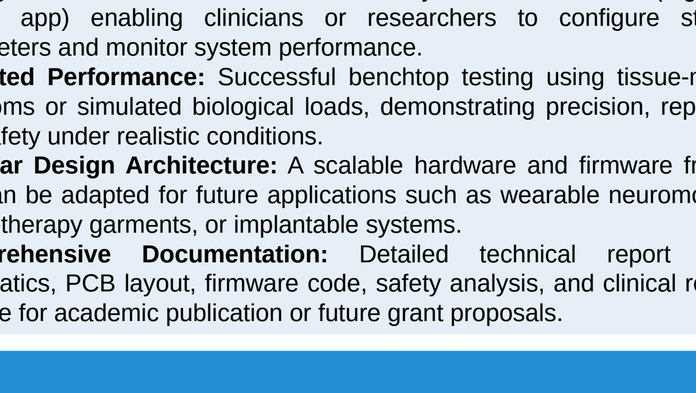
Anticipated Best Outcome

- **Functional Prototype:** A robust, multi-channel electrical stimulation device capable of delivering safe, programmable biphasic pulses with real-time control over amplitude, frequency, and waveform shape.
- **Intelligent Control Interface:** A user-friendly software interface (e.g., GUI or mobile app) enabling clinicians or researchers to configure stimulation parameters and monitor system performance.
- **Validated Performance:** Successful benchtop testing using tissue-mimicking phantoms or simulated biological loads, demonstrating precision, repeatability, and safety under realistic conditions.
- **Modular Design Architecture:** A scalable hardware and firmware framework that can be adapted for future applications such as wearable neuromodulation, electrotherapy garments, or implantable systems.
- **Comprehensive Documentation:** Detailed technical report including schematics, PCB layout, firmware code, safety analysis, and clinical relevance, suitable for academic publication or future grant proposals.

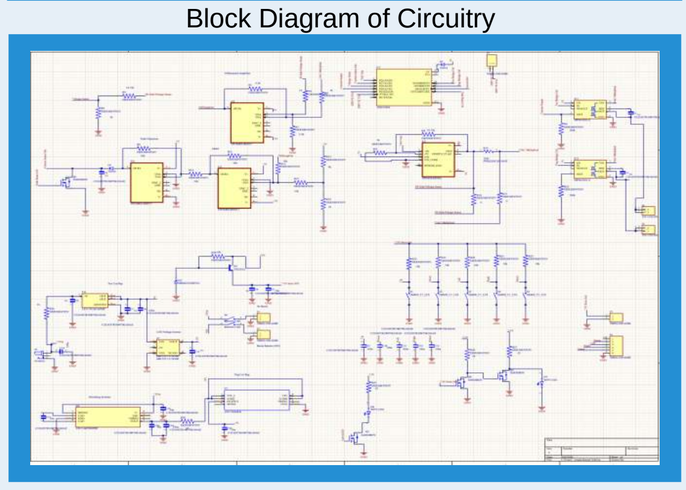
Project Outcome

The ElectroStim is a modular design capable of providing charge balanced biphasic pulses between 50uA and 50mA for biomedical research purposes

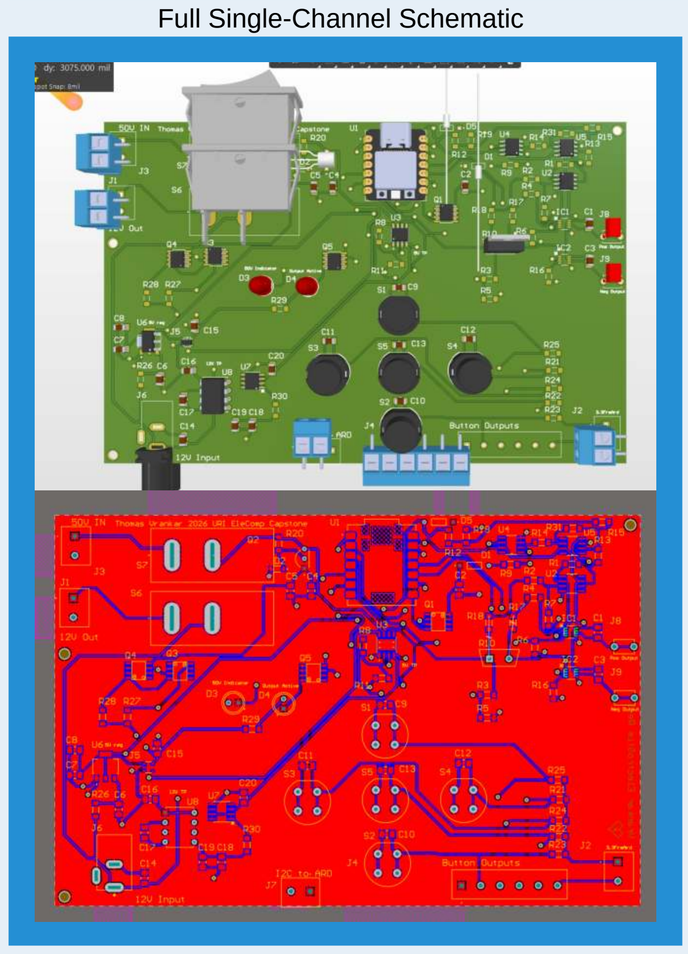
Figures



Block Diagram of Circuitry



Full Single-Channel Schematic



PCB Layout

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Remote Control

Remote Power Control/Monitoring and Solid-State Protective Devices for Electronic Systems Power Distribution Units

Team Members: Danny Haigh (ELE), Rafael Heagney (ELE), Robert Schmitt (CPE)

Technical Director(s): Matthew Huestis, Mike Brawner, Mike Brown

Project Motivation

This project looks to design a reconfigurable DC power distribution system for servers and electronic racks, with the overall goal of allowing students to assess technology options, build simulations, and fabricate a working prototype. The scope of the project includes rack-level DC distribution, power monitoring, consumption, data communications, and solid-state protection to deliver clean and reliable power distribution. Students will perform trade studies, evaluate Technology Readiness Levels (TRLs), and identify maturity risks, gaining experience from concept through prototype and test.

Anticipated Best Outcome

The functional specifications of the anticipated best outcome consist of physical and simulated models as follows:

1. A student-built non-functional prototype of a 400/12 VDC Power Distribution Unit (PDU) system with remote control and monitoring capabilities, used for visual spatial modeling.
2. A simulated 400/12 VDC Power Distribution Unit (PDU) portraying key functional behaviors representative of a full-scale, physically implemented system.

Key Accomplishments

Part Research and selection:

One aspect of this project was research for PDU systems. Power distribution systems and how to design Power Distribution Units were all aspects of our research. Once a foundation of knowledge was accumulated the beginning of part selection began.

Part selection was delegated to each team member and selection was determined based on a variety of factors including price, voltage rating, current rating, power rating, temperature rating, availability, country of origin, etc. Once enough information was gathered, decisions were made by each team member for which components would be used for the PDU design, utilizing technology readiness levels and Pugh decision matrices to aid in selection.

Block Diagram:

The block diagram is a basic overview of our design for the PDU. We have the high voltage stage, which deals with the input 400 VDC voltage to the system. High voltage is input and then the input protection follows before the filtering. After the input is filtered then we begin the low voltage stage, with DC-DC conversion. This stage handles very high current, so there are branch breakers and fuses along with output control relays. Finally, the output receptacles for the load of the system. The control side works in the background throughout each stage in the system, monitoring input and output stages, while also being in control of relays and breaker switches.

Simulations:

In Simulink we created a schematic of our design in order to test important cases. We wanted to insure protection capabilities of our design, in which we tested overvoltage and overcurrent cases. Parts that were selected had efficiency so powerloss cases were tested.

Building the simulated architecture also brought insight into how to properly interface the design. There are certain components required for interfacing, like decoupling capacitors for example, that were not foreseen before our simulations. The simulation also revealed that the system requires a pre-charge of the input filter to avoid high frequency transient oscillations upon turn on.

Prototype:

Due to lab and budgetary constraints we were unable to create a functional prototype, but we decided to build a nonfunctional prototype. The purpose of the nonfunctional prototype is to portray a visual representation to guide in future follow-up research and aid in a visualization of our specified architecture. Parts that were selected before were stepped down to facilitate a lower power requirements due to budget constraints.

Project Outcome

The team met both ABOs a non-functional physical prototype and a Simulink simulation validating overvoltage and overcurrent protection

Figures

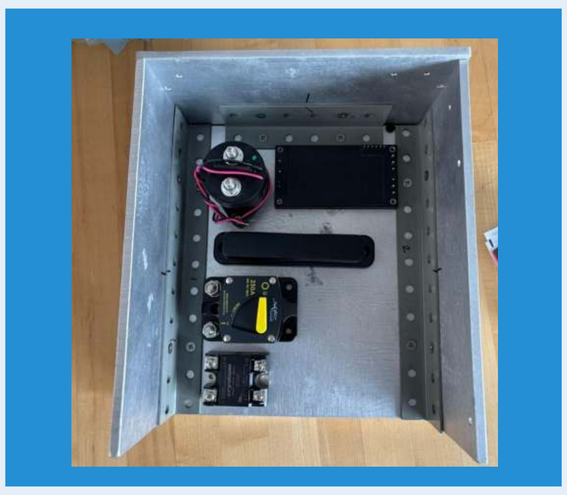

Figure 1: Non-Functional Physical Prototype

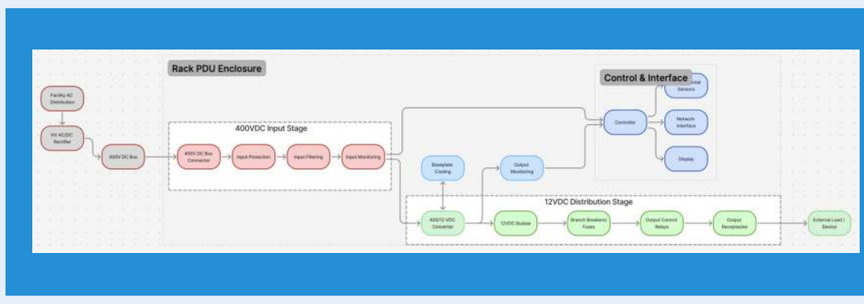

Figure 2: Block Diagram of PDU System

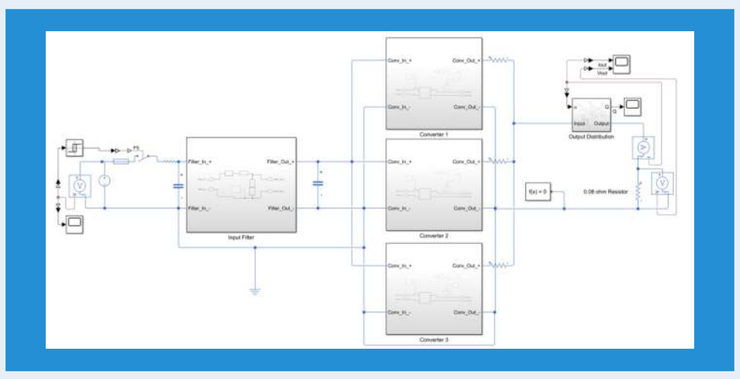

Figure 3: Simulink Simulated Architecture

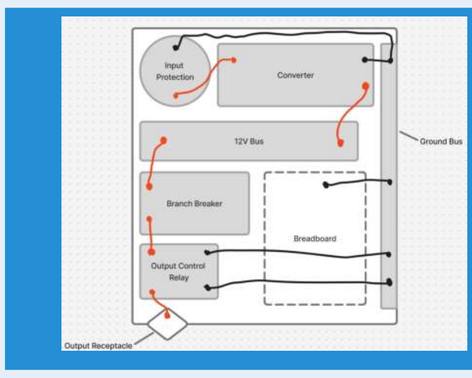

Figure 4: Physical Architecture Layout

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Shipyard 4.0

Cyber-Physical Testbed, Digital Twin, and Operator Dashboard for Secure Shipyard Manufacturing

Team Members: Aryana Sadr (ELE), Garrett Kemper (ELE/CPE), Laila Ghazi (ELE), Connor Sheridan (ISE), Juan Lopez (ISE), Nicolas Keegan (ISE)

Technical Director(s): Anissa Elias, Stephen Eacuello, Alexander Moulton, & Thomas Santos

Project Motivation

The U.S. currently builds less than 1% of the world's commercial ships, which shows how urgently the country needs to improve and modernize its shipbuilding industry. The April 9, 2025 Executive Order directly responds to this problem by pushing for stronger shipyards, a better trained workforce, and major upgrades in technology to help restore America's maritime strength. However, bringing new technology into shipyards also creates bigger security risks that must be addressed. This is where Rite-Solutions is in a strong position, because the company can lead research and development focused on supply-chain security, infrastructure protection, and resilience for future shipyard systems.

Key Accomplishments

Overall Key Accomplishments

- Subsystems integrated via ROS 2 nodes and topics. **(Fig. 5)**
- PostgreSQL database logging of test events.
- Modular, configurable, and scalable subsystem architecture.

Physical Testbed Key Accomplishments

- Testbed replicates core shipyard processes. **(Fig. 4)**
- Physical layout and system component identification. **(Fig. 1)**
- Trained computer vision models for real-time part identification and tracking.
- Integration of conveyors with ROS2 nodes.
- Power distribution for testbed.
- Electrical blueprint (KiCad) development.

Digital Twin Key Accomplishments

- Real-time modeling and simulation. **(Fig. 2)**
- MuJoCo physics engine with tuned contact dynamics.
- ROS 2 node structure.
- Configurable YAML and XML based architecture.
- Simulation of Niryo Ned2 and Xarm Lite6 robotic arms.
- Robotic pick and place of components.
- Rigid body collision detection.
- Dynamic part inventory management and lifecycle tracking.
- Component placement comparison and validation.
- Visualization of machine states.
- Review of past events through PostgreSQL database.

Dashboard Key Accomplishments

- Multi-panel UI for system topology, alerts, sensors, and cycles. **(Fig. 3)**
- Real-time monitoring of robots, conveyors, sensors, and machines via ROS 2.
- FastAPI-based backend with responsive web frontend (HTML/CSS/JS).
- PostgreSQL integration for logging and historical data analysis.
- Search and filtering of past events by device, category, and time.
- Scalable architecture for future analytics, alerts, and camera integration.

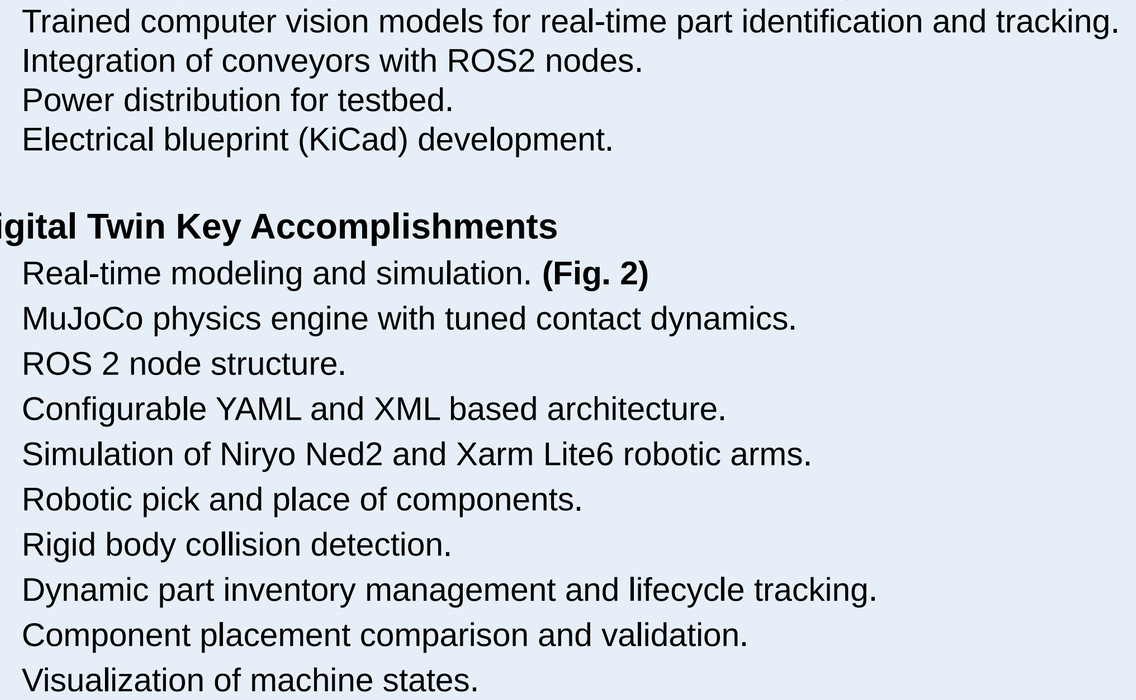

Fig. 5: ROS Network Architecture Diagram

Anticipated Best Outcome

Our best outcome is a fully integrated platform that improves the security and resiliency of shipyard manufacturing using a physical testbed, digital twin, and operator dashboard. The testbed of robots, conveyors, sensors, laser engraver, and CNC machine will run an automated workflow, while a ROS2/MuJoCo digital twin mirrors it in real time. The dashboard will monitor and control the system, visualize events, and support kill chain–based vulnerability analysis.

Project Outcome

The project is successful in meeting its anticipated best outcome. The physical testbed, digital twin, and operator dashboard integrate together to represent an automated shipyard workflow and provide insights and metrics to the user.

Figures

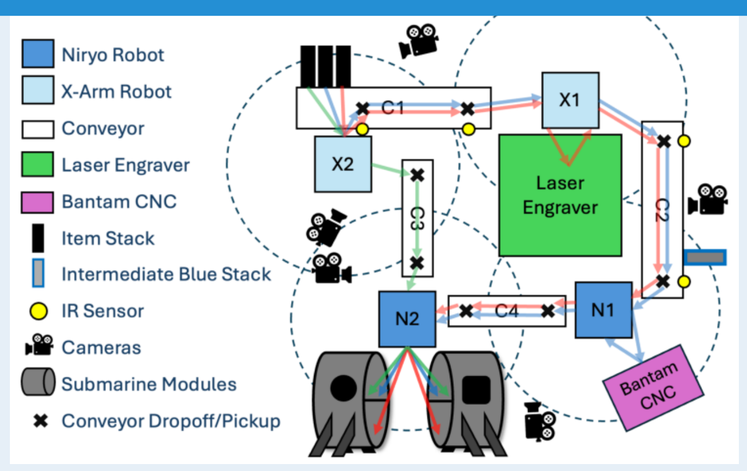

Fig. 1: Layout Diagram of the Physical Testbed

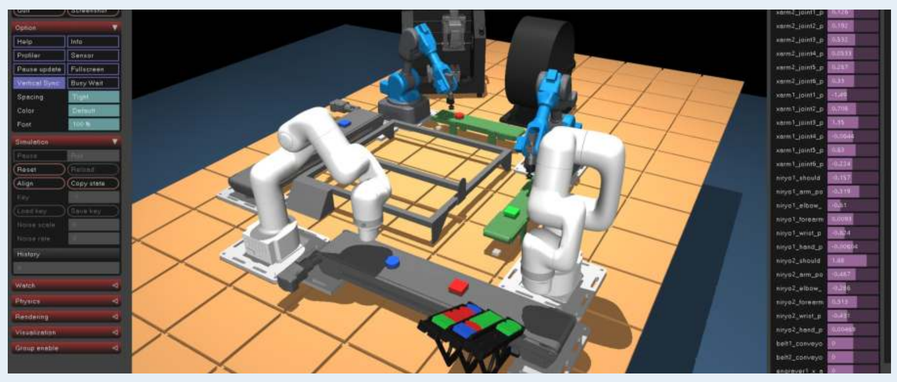

Fig. 2: Screenshot of the Digital Twin

Fig. 3: Screenshot of the Operator Dashboard

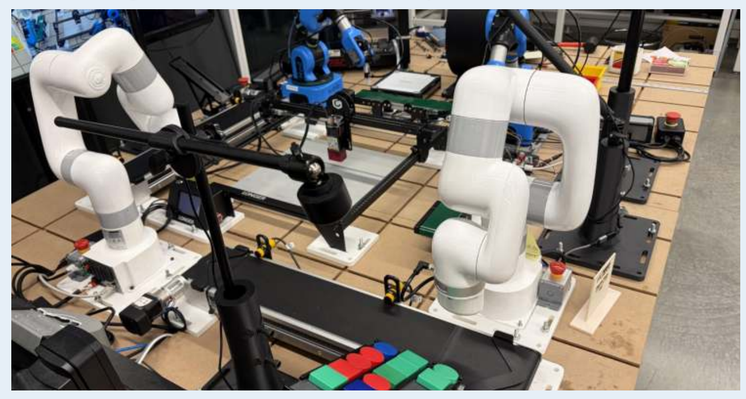

Fig. 4: Photo of the Physical Testbed

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URI ICRL RoboToy

A Robotic Toy for K-12 Robotics and Programming Exposure

Team Members: Joseph Rose (CPE), Jack Petrarca (ELE), Gage Testa (ELE), Cade Birrell (ELE)

Technical Director(s): Dr. Paolo Stegagno, Cameron Amaral

ICRobots Intelligent Control and Robotics Lab

Project Motivation

Exposure to computer science at a young age can promote social equity by increasing representation and access to technology careers. Developing programming skills early can open pathways to well-paying jobs, helping provide long-term financial stability for marginalized groups that have historically lacked such opportunities. Greater participation from under-represented communities also enhances diversity in computing and helps expand the overall STEM workforce. The ICRobots Lab is partnering with the URI College of Engineering to deliver robotics-focused STEM programs to Rhode Island's most diverse K–12 schools. However, tools designed for teaching programming and robotics in early education (K–5) remain limited. Young students are still developing basic reading and math skills, which makes traditional programming—even in graphical form—difficult, especially when it relies on computers, mice, and keyboards. These tools also lack the hands-on, manipulative experiences essential in early childhood. Creating new robotics platforms tailored for early learners will help bring high-quality STEM education to the communities that need it most.

Key Accomplishments

Li-Ion Battery Charger:
The Li-ion battery charging subsystem design has been completed and integrated into the full-scale RoboToy PCB with minor refinements. Prototype testing identified inefficiencies, including suboptimal inductor selection; this was corrected by selecting a value better matched to the converter's operating conditions. The boost converter leverages integrated feedback control, improving regulation performance while reducing external component count and overall system cost. Updated component selections for the battery fuel gauge and Li-ion charger ICs were made to improve manufacturability and ease of assembly, thereby reducing the risk of soldering-related defects without impacting system performance.

PCB
The PCB design has been completed and includes all of the necessary features outlined by the ABO. The board has successfully implemented the button array, motor driver, ESP 32, Ultrasonic sensors, buzzer, microphone, and rechargeable battery. Version 1 of the design consists of push buttons for the array while Version 2 has pogo pins for better contact with the physical programming blocks. Version 1 can be seen in Figure 1. The top left of the board contains the battery charging ICs and ports while the middle contains the button array, and the right side consists of the buzzer, microphone, motor driver, and one of the ultrasonic sensors.

Button Array and Pogo Pin Array:
Both the button array and pogo-pin array use a row–column matrix with pull-up resistors to maintain a default logic high on each line. A button press or conductive bridge connects a specific row–column intersection to ground, producing a logic low. The ESP microcontroller detects individual inputs by sequentially driving each row while monitoring the column lines. During scanning, if a connection is present at a given intersection, the corresponding column reads low, allowing precise identification of the activated button or contact point. Using this, specific sequences of inputs can be mapped to actions such as moving the RoboToy or generating sounds. This is implemented through interchangeable blocks placed on top of the RoboToy, which either use a foam tip to create a press or a conductive strip to complete connections across the pogo-pin array. The pogo pins themselves are spring-loaded contacts selected for their compact size and reliable electrical interface, with a typical stem diameter of approximately 1.1 mm and a corresponding pad size slightly larger to ensure consistent contact. Their travel distance and spring force allow them to maintain connection even with minor misalignment, which is important for repeatable performance. Proper spacing and alignment of these pins on the PCB were critical to ensure that each row–column intersection is accurately addressed without shorting adjacent contacts. A schematic diagram is shown in Figure 2 to help demonstrate the architecture of the button array.

Programming of RoboToy Microcontroller:
System integration has progressed to a functional state, with the ultrasonic sensors, motor driver, and buzzer operating correctly under program control. Current development focuses on implementing reliable input handling for the button array and mapping inputs to programmable behaviors. Each programming block is interpreted using an opcode-based approach, where specific input combinations correspond to predefined instructions that determine system response. Communication between components is supported through the use of I2C, enabling efficient and organized data transfer between the microcontroller and peripheral devices while minimizing required wiring and pin usage. Optimization efforts are being applied to the scanning routine. Since programming blocks remain static during operation, high-speed scanning is only required during insertion. After detection, the scan rate can be reduced or disabled, with periodic low-frequency polling used to detect block removal, thereby improving overall system efficiency. This approach also reduces unnecessary bus activity and processing overhead, contributing to more stable and predictable system performance during continuous operation, even under varying input conditions and extended runtime scenarios.

Anticipated Best Outcome

The Anticipated Best Outcome (ABO) of this project is a fully functional single-board prototype that integrates the ESP 32, motor driver, and input buttons. The board must fit inside the robot's body, read 8 rows of 8 buttons, two IR sensors, and a microphone, while also driving motors and producing sound. Powered by a Li-Ion battery, the robot will read a sequence of 8 blocks representing code lines, with up to 16 visually distinct commands, including movement, sound, loops, and conditionals. Additional features include obstacle warnings and sound-based reactions. Firmware will follow a Finite State Machine structure for reliability and debugging.

Project Outcome

The Robo-Toy Team was able to meet the largest goal of creating a fully integrated PCB design. However the programming blocks and 3D printed housing need more development.

Figures

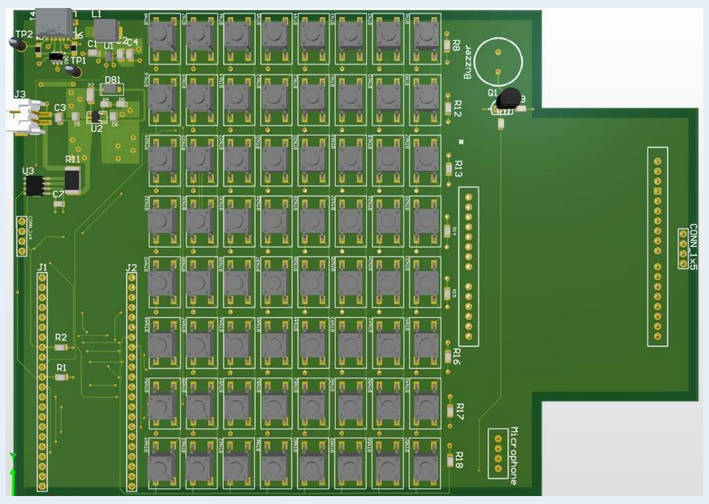

Figure 1: Robotoy PCB 3D render

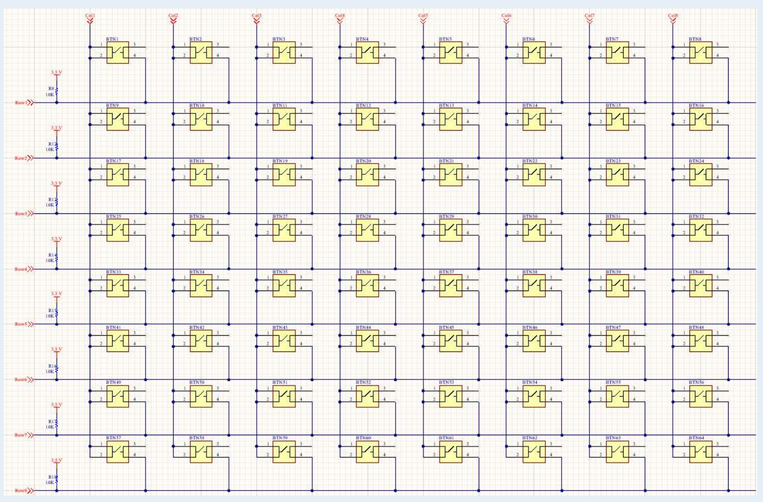

Figure 2: Button Array with Row pull up Resistors

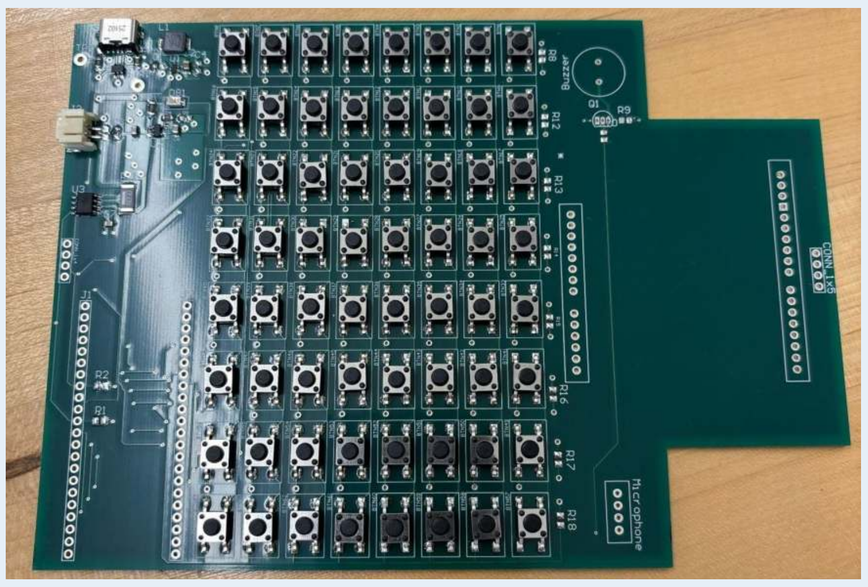

Figure 3: Physical PCB Assembly of Version 1 with headers not in place

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SANCTUARI ALPHA INDIA 2

Team Members: Jackson Albro (CPE) and Grey Daly-Labelle (ELE)

Technical Director: Joe Moreira **Consulting Technical Director: James DeMello**

SANCTUARI
A 501(C)(3) NONPROFIT ORGANIZATION FOR WILDLIFE

Project Motivation

Within the field of wildlife rehabilitation, there is a need to monitor the animals that are being rehabilitated, whether that be through traditional means or with new technologies. At the SANCTUARI rehabilitation center, animals are monitored with a multitude of security camera systems that trigger whenever they detect motion. While this feature is helpful for the rehabilitators, there are many occasions of a “false positive” motion or a non-animal being captured on video, taking up unnecessary disk space. Over time, much of the video data captured by the security cameras may be unhelpful for further use. As the team assigned to this project, our task is to implement a system that uses object recognition and AI to filter out the “false positive” video data and create a reliable set of animal data. When this objective is achieved, the refined data can be further processed with AI tools in order to classify animal behaviors and movements that will be useful in conservation and rehabilitation efforts.

Anticipated Best Outcome

Within this project, there are seventy-five (75) ABOs, however we only have to complete twenty-five (25) of these ABOs to achieve a successful project. The first third of the ABOs are what we have been focusing on thus far, and they involve implementing a filtering method in order to process large amounts of video data in a timely and reliable manner. The rest of the ABOs deal more with the continued processing of the refined data, namely the use of AI tools to classify animal behaviors and movements.

Key Accomplishments

- **Object Detection/Classification Selection:** Early on within the project, we were fortunate enough to find pretrained AI models that could be used to complete some of our ABOs. The primary model that we have been utilizing thus far, Google’s camera trap AI, includes generous amounts of documentation and was straightforward in setting up and testing on our local system. The camera trap AI accepts images as input, and outputs detection and classification files for each batch processed, revealing what was found in the input. We also found another model that can possibly be used for redundancy purposes, but so far it has proved to be less reliable than the camera trap AI.
- **Construction of Processing Pipeline:** As the project progressed, there was a need to determine the components that would need to function at each stage of the data processing/filtering pipeline in order to receive a usable output. Given that the primary detection/classification tool that we are using only accepts images, a component to split videos into frames was necessary to add into the processing pipeline. Over time, this pipeline would be refined and developed to be more robust and to include multiple layers of object detection **(see fig. 1)**.
- **Development of Processing Interface:** In the second semester, a more featured processing interface was developed in order to make the processing pipeline more streamlined **(see fig. 2)**. The interface is written with the PySide6 library in order for the application to be fully usable in the desktop environment. The interface can complete the same tasks as its predecessors, but it is far more robust and also gives the user additional features, such as process cancellation, built-in frame sampling selection, and face blurring for human detections. The user also has the ability to switch between detection models within the interface (currently YOLO and Megadetector).
- **Development of Visualization Interface:** In the second semester, work was done on developing an interface for viewing post-processing detection results **(see fig. 3)**. This interface allows the user to visualize detection data for a given video. When the user chooses their desired videos, the application will let the user view the detection scatterplots for the chosen videos. The user can also adjust the confidence level and detection category to change what appears in the scatterplot. It is important to note that the scatterplot aggregates all detection data from all frames initially, which can then be filtered by the user by setting the confidence level and detection category. From there, the user can click on the scatterplot to view the data for Megadector and the three YOLO models. The user can also overlay the four graphs visually, view frames that the models agreed on, use a range selector to find frames in a given range, or hover over points on the graph to view frames, among other features.
- **Use of Detection Density Map:** Within the visualizer interface the user can select a video like normal and create a density map that shows where the densest set of detections are within the video **(see fig. 4)**. This is especially useful because this data can be used to create masking over false positives so these detections do not repeat themselves in later videos. This works under the assumption that animals move around a lot and therefore have a more spread out detection range so the density points of actual animal detections is a low percentage.

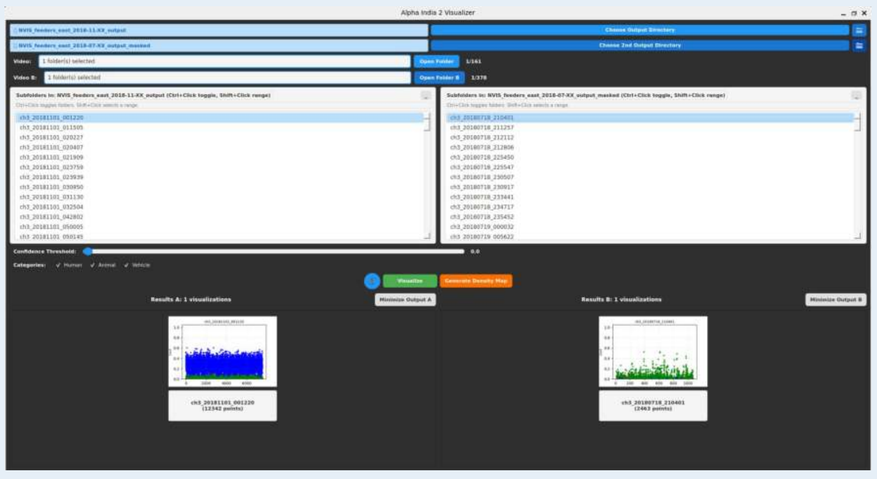

Fig. 3: Screenshot of visualizer user interface

Project Outcome

The project consists of seventy-five (75) ABOs, of which only twenty-five (25) are required for successful completion. The initial third of these ABOs are focused on implementing an efficient filtering method for processing large volumes of video data. This has been completed using MegaDetector, along with a custom user interface (UI) as illustrated in figure 1 and 3. Thi s implementation enables reliable and timely reduction of raw video data into a refined subset suitable for further analysis.

Figures

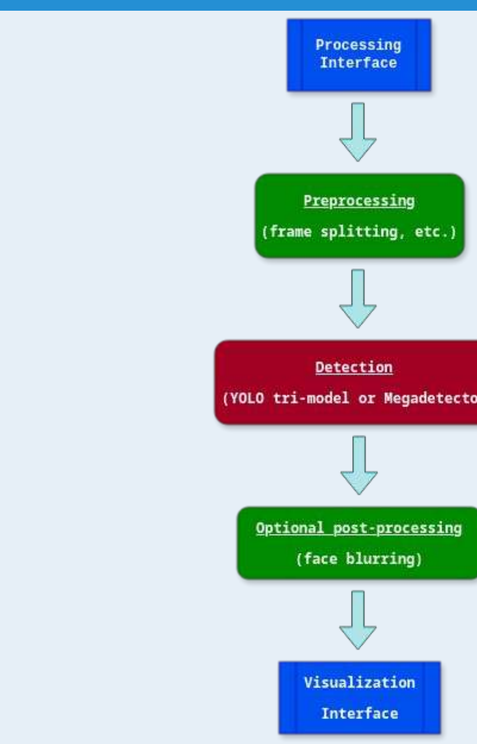

Fig. 1: Flow diagram of processing pipeline

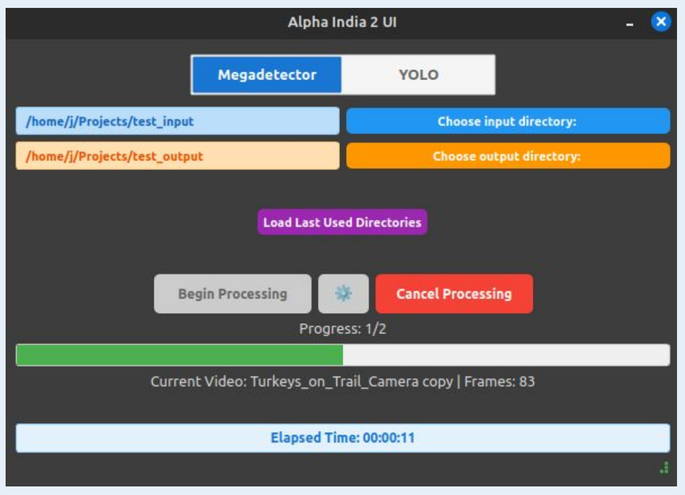

Fig. 2: Screenshot of processing user interface

Fig. 4: Screenshot of detection density map created in the visualizer user interface

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Echo Mike 3

Post-Release Tracking Device for Small Mammalian Species

SANCTUARI

Team Members: Cam Farmer (ELE), Sophie Plante (CPE), Douglas Fischer (CPE & ELE)

Technical Director: Joe Moreira

Project Motivation

Rehabilitators rarely receive post-release updates on animals, creating a major gap in understanding survival and rehabilitation success. SANCTUARI saw tracking technology as a solution. Echo Mike 3 delivers a small, low-power, affordable tracker built specifically for species like foxes, raccoons, and rabbits. Its design supports SANCTUARI's mission to improve wildlife welfare and expand knowledge of post-release behavior. By enabling consistent, real-world data collection, Echo Mike 3 helps bridge the gap between rehabilitation efforts and long-term outcomes.

Anticipated Best Outcome

Successful design, prototyping, and testing of a small, lightweight, wearable, long-service-life tracking architecture (electronics and battery power source) suitable for smaller mammalian species such as foxes, raccoons, skunks, opossums, rabbits, and more. A "stretch goal" is to include smaller species should the basic architectural design be suitable.

Key Accomplishments

Embedded-Cloud Integration: Completed full end-to-end communication between firmware, mobile application, and Appwrite backend. Defined a structured JSON telemetry schema (GPS, battery, timestamps) and implemented BLE-based data exchange between the BG24 device and Flutter app. Configured Appwrite collections, authentication, and permissions, and built a secure ingestion pipeline. Successfully validated the complete path from device → mobile → cloud with reliable storage and retrieval (Figure 2).

BLE Communication Framework: Developed a robust BLE communication system using structured JSON command/response messaging. Enabled bidirectional interaction for telemetry streaming, device status, and configuration commands. Resolved early firmware instability and ensured consistent notification handling, resulting in reliable real-time communication between embedded device and mobile application.

Auto-Log Scheduling System: Designed and implemented a flexible auto-log scheduler within the mobile app supporting both interval-based and user-defined scheduled logging. Integrated scheduler execution with live tracker telemetry to ensure accurate data capture. Validated the full pipeline from scheduler trigger → tracker fix → local history → Appwrite upload.

Mobile Application Development: Completed the Flutter application including architecture, BLE integration, and user interface. Implemented real-time and historical data visualization using OpenStreetMap, including a scrollable Tracker History system displaying timetamped location data (latitude/longitude) across recorded datapoints, with persistent storage and interactive map views. Ensured smooth navigation, responsive UI updates, and consistent data synchronization across screens (Figure 4).

User Experience & Reliability: Finalized usability features including Settings configuration, auto-log controls, and authentication flows. Implemented a secure in-app password change feature and a support-based password recovery system. Added debug instrumentation and validation across the system to ensure reliability, traceability, and correct end-to-end behavior.

Board Design: The PCB testing board design was completed in such a way to allow for the maximum amount of modularity and design corrections. Though this choice made the testing board significantly larger than the final designs size constraints, the manufactured layout has the capability to have other evaluation boards, such as a battery fuel gauge component board, connected into the testing board and integrated into the design. Additionally, a preliminary production board design has been completed, and is ready to have additional components such as the battery fuel gauge implemented into the design (Figure 3).

Board Testing: All components, traces, and signal corrections have been tested on the PCB testing board. All apparent design errors made in the previous team's design have been corrected, and all that remains is to implement the firmware, test the antenna connection and communication, and the data storage in the MCU.

BG77 Replacement Selection: Upon discovering the excessive power consumption of the BG77, a replacement IoT module was needed. After reviewing designs and reference manuals of eleven other IoT IC components, the Nordic nRF91 was chosen based on several criteria. Not only does the nRF91 use significantly less power overall and when powering LTE communication, but a stripped down version of the IoT module is scheduled for release this summer, which will provide further power saving measures and reduced size. Additionally, the nRF91's firmware code's syntax structure mirrors the BG77's with comparable function libraries. This should ease the transition between the BG77 and the nRF91 when testing communication. Finally, the nRF91's evaluation board was the most comprehensive, and the connections needed to be made to integrate the nRF91 into the PCB testing board have been determined and are ready to be implemented once testing with the BG77 is complete.

Project Outcome

Core hardware functionality was confirmed, and firmware testing is now in progress. A working cloud backend and mobile application has been developed, providing reliable data storage, communication, and visualization. These results position the system for full integration and refinement in the next phase.

Figures

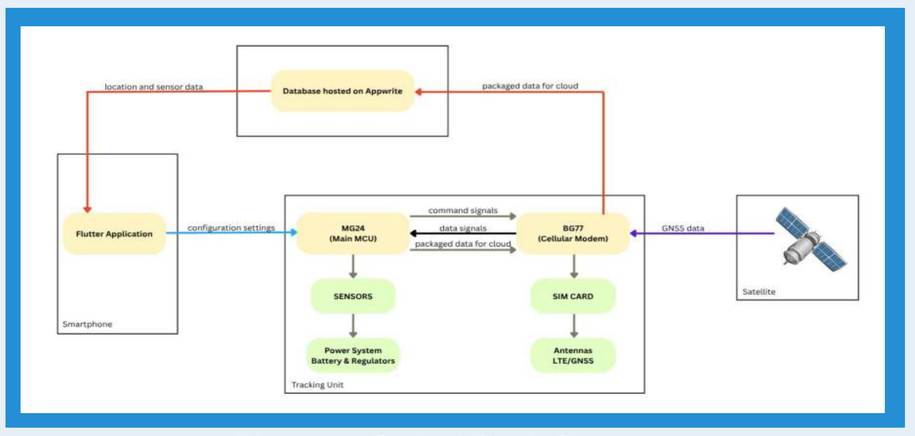

Figure 1: Project Block Diagram

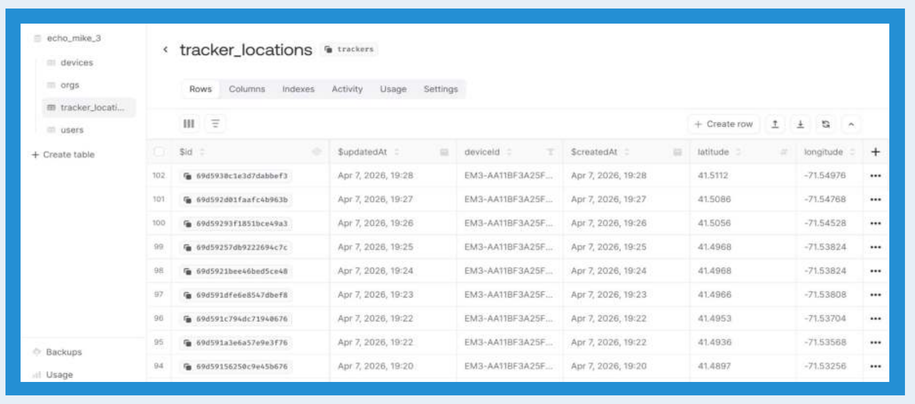

Figure 2: Appwrite *tracker_locations* Collection

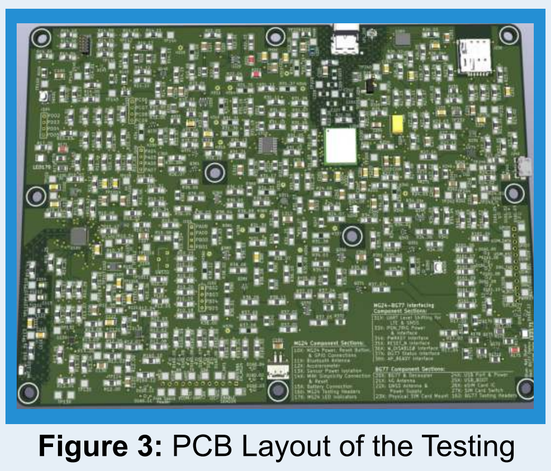

Figure 3: PCB Layout of the Testing Board

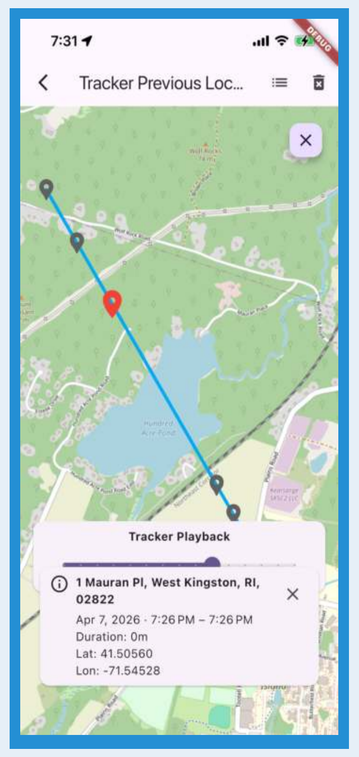

Figure 4: Tracker Previous Location Screen (Map View)

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Hybrid Crossover Zone Valve

A smart, Self-Powered Valve Improving Hot Water Efficiency

Team Members: Owen Morelli (ELE/MCE), Gabriel Arabik (CPE), Maxwell Gleadow (ELE)

Technical Director(s): Adam Bouchard, Nicholas Costello, Aaron Hertzer CTD: Mike Smith

Project Motivation

The Smart valve project aims to reduce water waste during heating cycles. This could not only lead to massive improvements in domestic water usage, but also result in energy savings while reducing wear on hot water heaters. This would be ideal for areas that suffer from water shortages. Creating an automated self-powered system has the potential to influence both residential and commercial standards, potentially leading to major energy savings. The Hybrid Crossover Zone Valve is a proof of concept, exploring the growing field of IoT devices and self-sustainable technology. In this way, success in this project would indicate potential for further investment in similar lineless smart home devices making use of energy harvesting technologies. Ultimately the Hybrid Crossover Zone Valve is conducive to forward-thinking engineering taking a step towards developing more efficient and intelligent systems available to residential homes.

Anticipated Best Outcome

We aim to develop an autonomous, lineless hot water crossover valve. An integrated MCU, actuator, and sensors serve to intelligently keep hot water at the valve for faster hot usage at the tap. The MCU will take in sensor data and run through predetermined procedures and logic in order to autonomously stroke the valve by usage of the actuator. This will be powered solely by energy harvesting methods to keep our product completely lineless and batteryless. We will create a first revision development kit that allows for further testing and research by switching between two modes: programming, and lineless testing.

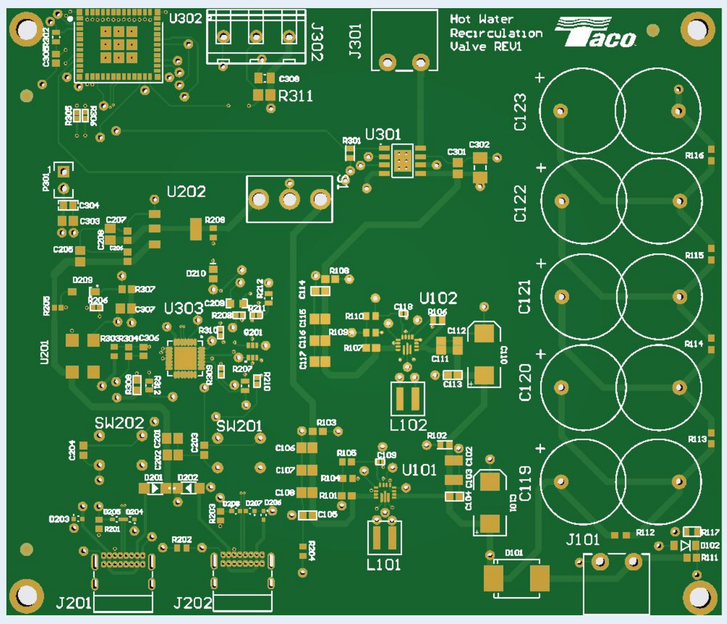
Key Accomplishments

REV1 DevKit: A first revision development kit was designed to evaluate the feasibility of the proposed lineless system (**fig 1**). This PCB integrates a 1F super capacitor bank rated for 27.5v, this is regulated to 3.3v to power our MCU and digital temperature sensors, an additional boost-buck converter is used to provided 5v for the purpose of powering our motor driver. A SPDT switch is located in the center of the board to convert from programming and debugging to lineless power operation. Switching to debugging allows for the MCU to be flashed, and for software to be tested by providing 5v via usb which is stepped down via a linear regulator. Test points for every net are accessible on the backside of the board for ease of hardware troubleshooting.

Energy Harvesting: A supercapacitor power bank was developed to supply power to the system. This was achieved by connecting five 5F capacitors in series and stabilizing the bank with high-precision balancing bleed resistors. The bank can be charged using an inline turbine capable of producing approximately 12v under typical sink flow conditions. System feasibility was validated through charge and discharge testing. As shown in **Fig. 3**, the bank reached 2v (the minimum input voltage of the boost-buck converter) in approximately 30 seconds, 5v in about 90 seconds, and near full charge in roughly 800 seconds. Discharge testing was also performed for multiple capacitance values. The 5F configuration outperformed all others, requiring approximately 160 hours (6.5 days) to fall below the 2v operating threshold, as shown in **Fig. 2**.

Sensor Intergration: Several sensors are integrated in the REV1 design among them: a digital temperature sensor, voltage monitoring on our super capacitor bank, and current sensing on the H-bridge motor driver. Voltage monitoring allows for the MCU to determine the flow rate of the sink. Current sensing is used to indicate the position of the valve. A temperature threshold may be set to determine when valve acautation occurs.

Control System Logic: The MCU goes through a simple process to control the valve. The MCU checks the current temperature of the water at the valve. If the temperature is to low, then the valve sends a BLE advertisement and a notify signal when a connection is made to the circulator to call for hot water via a data packet. This packet contains the current temperature of the water at the valve, the amount of time the circulator should run for, and a call for hot water. The MCU opens the valve for the duration of this process. Then the MCU calculates a dynamic deep sleep timer and closes the valve when the cycle is complete and goes into a deep sleep for the allotted time. If the temperature is within acceptable limits then the MCU calculates the dynamic deep sleep timer and goes back to sleep.



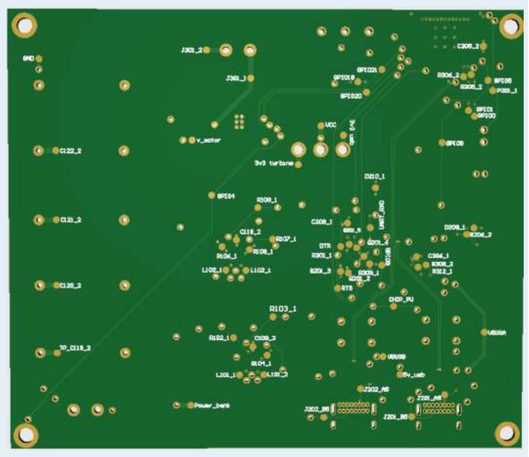


Fig. 1 Hot Water Recirculation Valve REV1 PCB

Project Outcome

The original ABO was not fully achieved, continued research revealed additional technical complexities beyond the initial project scope. As a result, the project direction evolved and a REV1 development board was designed to further investigate and validate the system.

Figures

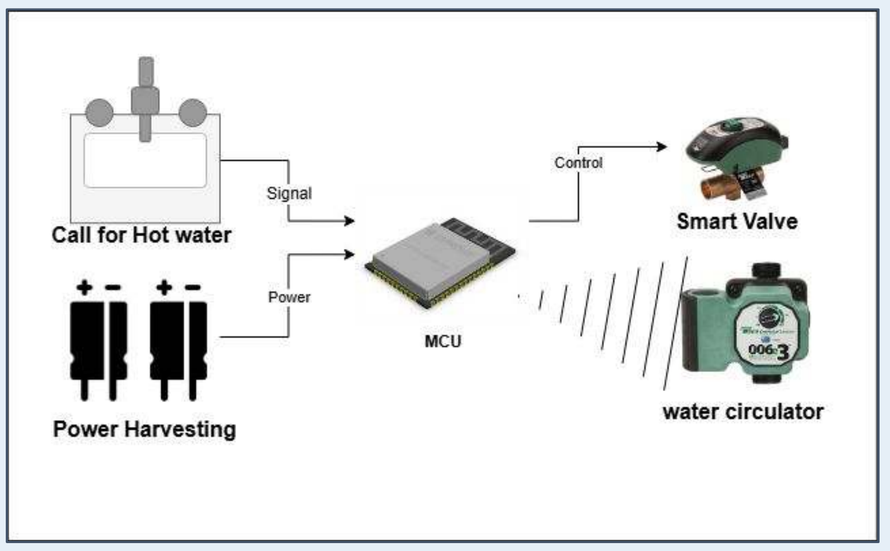


Fig. 2 Project overview Block diagram

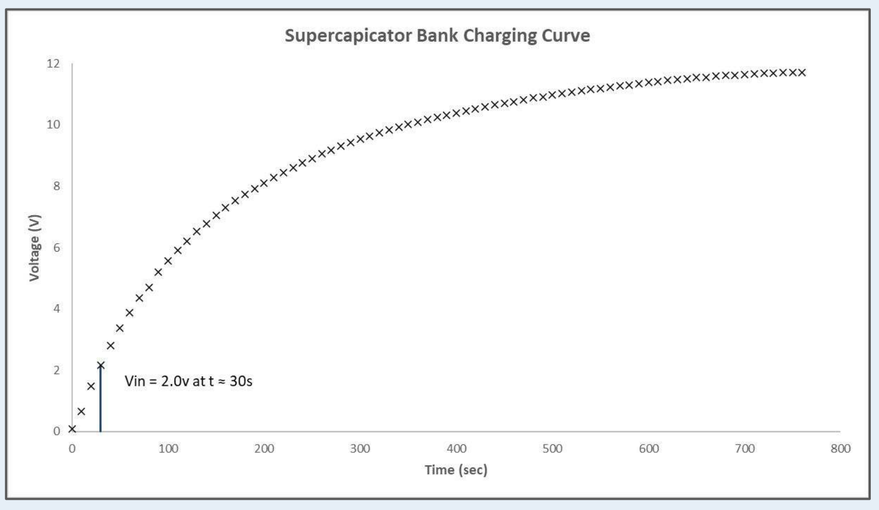


Fig. 3 Supercapicator charging curve

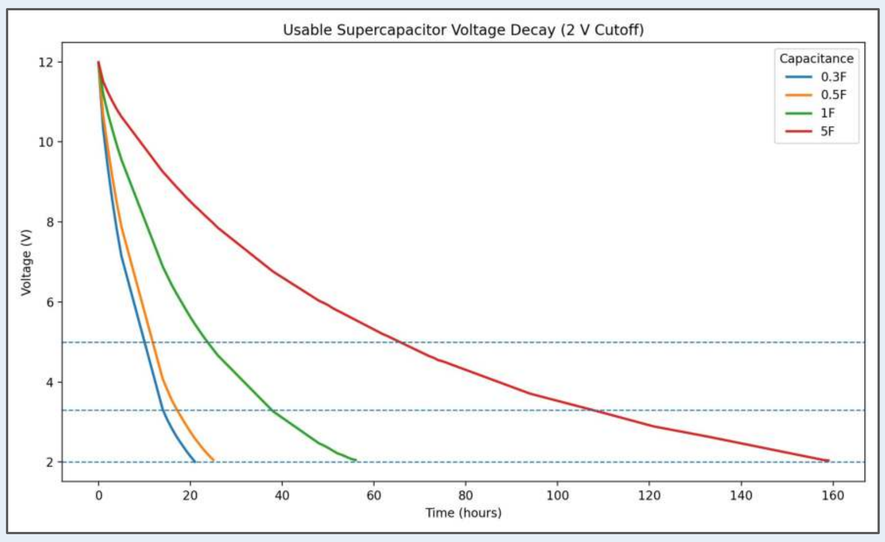


Fig. 4 Supercapicator discharging curve

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URI CYPHER Center

Real-Time Detection of Man-in-the-Middle Attacks in Industrial Control Systems Using Network Traffic Analysis

CYPHER Cyber-Physical Intelligence and Security

Team Members: Milan Koshy (CPE), Alejandro Wu (CPE), Ricky DiMare (ELE), Isaac Feldmann (ELE), Jacob Lee (ELE)

Technical Directors: Dr. Hui Lin, Meem Tasfia Zaman, Jake Nicynski, Zack Notarianni

Project Motivation

Industrial control systems like power grids present a unique cyber-physical infrastructure to collect measurement data and perform control operations to ensure continuous stability. From traditional power systems to recent smart grids, communications networks are critical in sharing information in this domain. Even though they use similar technology to the public Internet, industrial control communications networks serve unique applications, i.e., sharing information related to physical processes and delivering control commands to maintain their stability. The features add new ingredients to infrastructure and network protocols used by smart grids, which malicious actors can leverage to launch cyber attacks that aim to disrupt smart grids' physical processes. Unlike cyber attacks targeting general-purpose computing environments, cyber attacks targeting critical industrial control systems introduce unrecoverable consequences, including power outage, economic losses, and even human casualties.

Key Accomplishments

- **Construction of example circuit:** An example circuit was built using a 3.3k ohm resistor, LED, and a MD-D262 circuit breaker. This circuit is powered by a raspberry pi after establishing the connection to the circuit. This will allow us to code the LED to switch on and off at a certain rate. The following image will display the circuit along with the raspberry pi.
- **SEL-751A Relay:** The manual for the SEL-751A relay was the first step in setting up and configuring it. Next the SEL-751A relay was set up and configured using the acSELerator quickset. The relay is being used as a switch when connected with the example circuit. The relay is being controlled through ethernet connection to a PC from the relay.
- **DNP3:** DNP3 was used as the communication protocol between a Raspberry Pi acting as the master and an SEL-751A Relay acting as the outstation. The protocol allowed the Raspberry Pi to send control commands and read status information from the relay over a TCP connection. Using a Python implementation of the protocol, the system was able to issue control relay output block (CROB) commands to toggle specific relay bits and perform polling to monitor relay states, enabling remote control and monitoring of the relay through the network.
- **MITM Attack**: For our project, an ARP cache poisoning attack, also known as a man-in-the-middle (MITM) attack was conducted between the outstation relay and the master node. We used ARPSpoof, a command-line networking tool to carry out the attacks. When an attack occurs, it causes the master node to think the attacker machine is the relay, and the relay to think the attacker machine is the master. As both machines are sending network packets to the attacker machine instead of each other, the attacker is able to monitor all network traffic between the master and relay. This is known as packet sniffing.
- **Packet Modification:** In addition to packet sniffing, we took it one step further and modified the network packets between the relay and master. In this case, when the master sends the ‘on’ command, the relay would instead receive the ‘off’ command, and when the master sends the ‘off’ command, the relay receives the ‘on’ command. This was done through running a python script using the NetFilterQueue (NFQ) library. The python script filters out all network traffic aside from DNP3 packets, and analyzes the DNP3 packets for specific sequences of bits. If the python script identifies the sequence for ‘on’ or ‘off’, the script then modifies the corresponding packet.
- **RTT Tracker:** To track when a MITM attack may have occurred, we track the round-trip-time (RTT) of the DNP3 message and response. After an attack occurs, DNP3 packets first go through the attacker machine before heading to the relay, and responses go through the attacker before reaching the master, adding latency. By tracking the RTT of the DNP3 packets, if the latency increases we can reasonably guess that a MITM attack may be occurring. This was done through a python script on the observer machine, which monitors the RTT of DNP3 packets between the master and relay.

Anticipated Best Outcome

ABO1: A fully functional ICS including cyber-physical infrastructures. Objective: Enables students to obtain a fundamental understanding of cyber-physical interactions in today’s ICSs.

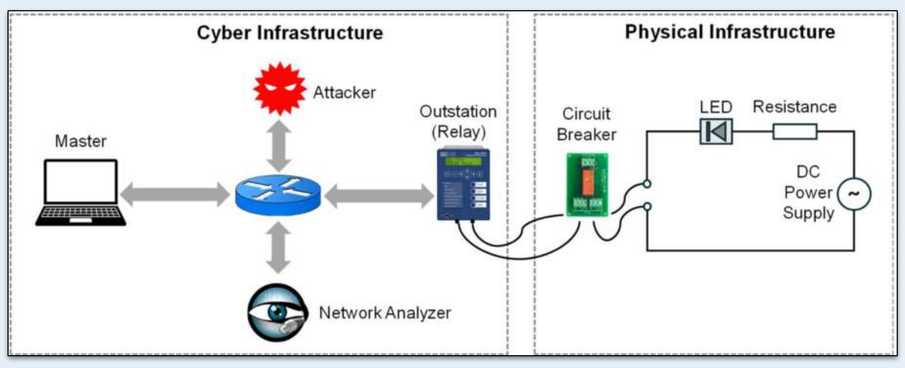
ABO2: A fully functional man-in-the-middle attack through compromising ARP caches in network nodes. Objective: Enables students to grasp the basic knowledge of cyber attacks in communication networks.

ABO3: A fully functional detection module that can detect the implemented man-in-the-middle attacks through network traffic analysis. Objective: Enables students to obtain in-depth knowledge of network traffic analysis, e.g., deep packet inspection.

Project Outcome

This project includes three (3) total ABOs. With the guidance of our Technical Directors, the team was able to successfully complete all three by the given deadline.

Figures



This is a block diagram of our project. To the left is mock cyber infrastructure where the DNP3 master, attacker machine, network analyzer and intelligent relay are connected through a network switch, while the right side shows the physical infrastructure modeling the power grid.

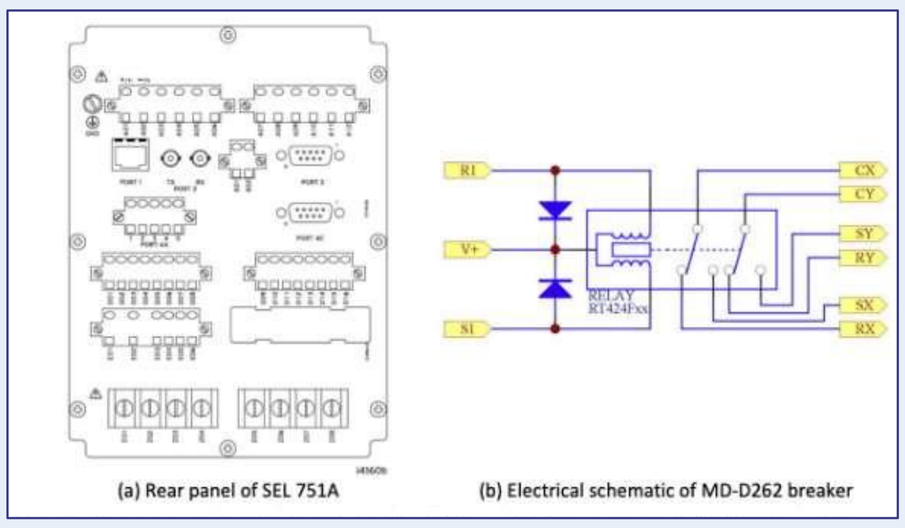
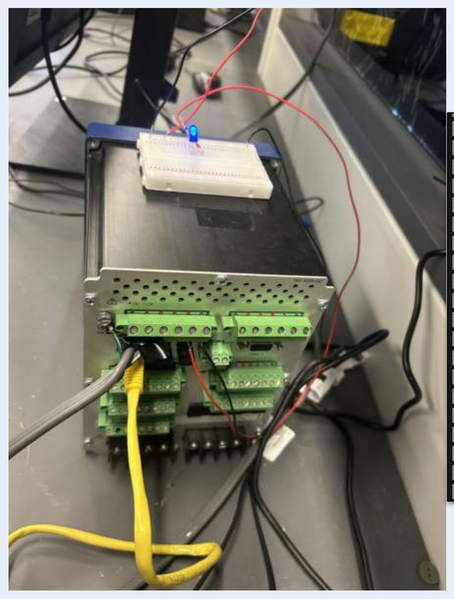


Figure showing the pinouts on the intelligent relay



```
[FUNCTION CODE]: 0x1
[FLOW] 192.168.10.7:20000 → 192.168.10.1:49535
[FLOW] 192.168.10.7:20000 → 192.168.10.1:49535
[FLOW] 192.168.10.1:49535 → 192.168.10.7:20000
[FLOW] 192.168.10.1:49535 → 192.168.10.7:20000
[FUNCTION CODE]: 0x5
[+] Direct Operate detected
[+] CROB found at byte 13
[+] LATCH OFF → ON
[+] Flipping control: 0x4 → 0x3
[+] Fixing CRC
[FLOW] 192.168.10.7:20000 → 192.168.10.1:49535
[FLOW] 192.168.10.7:20000 → 192.168.10.1:49535
[FLOW] 192.168.10.1:49535 → 192.168.10.7:20000
[FLOW] 192.168.10.1:49535 → 192.168.10.7:20000
[FUNCTION CODE]: 0x1
[FLOW] 192.168.10.7:20000 → 192.168.10.1:49535
[FLOW] 192.168.10.7:20000 → 192.168.10.1:49535
[FLOW] 192.168.10.1:49535 → 192.168.10.7:20000
[FLOW] 192.168.10.1:49535 → 192.168.10.7:20000
```

To the left shows an image of the physical hardware setup for our project, the intelligent relay connected to our sample circuit.

The image to the right shows the output of the MITM packet modification script. Here, we can see when a direct operatte command is identified, and the command is flipped.

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URI Power Electronics Laboratory

Innovative Design Automation Framework for integrated Power Building Blocks (iPEBB)

Team Members: Marc Delgado (ELE), Daeven Goel (ELE), Nicholas Rossi (ELE), Maximus Matarese (CPE)

URI PEL
University of Rhode Island Power Electronics Lab

Technical Director(s): Yeonho Jeong, Xueshen Zhang, Fuwei Li, & Sooan Pack

Project Motivation

Modern Power Conversion Systems (PCSs) are essential for efficiently delivering energy for electronic applications. However, their design process remains complex, time-consuming and require multiple iterations. To overcome long design process and development cycles of traditional PCS, the project aims to implement the integrated Power Electronics Building Block (iPEBB) framework. The iPEBB framework offers a scalable solution to unmanned aerial vehicle (UAV) applications that can meet diverse power requirements. Consequently, the benefits extend into the manufacturing field by accelerating the production of PCSs.

Anticipated Best Outcome

This project aims to develop two fully functional PCS designed for two different drone applications: 6-S hexacopter and 4-S quadcopter. The initial stage involves the design, implementation, and testing of a single iPEBB, capable of meeting the electrical requirements of a 2-S configuration. After successful evaluation, multiple iPEBBs will be integrated and tested to achieve the power rating of each drone, and ultimately assembled into the two drone platforms for final demonstration.

Key Accomplishments

1. Converter Topology Selection (LLC Resonant and Flyback Converter)

a) Topology Research and Selection

- Conducted comparative analysis of isolated DC-DC topologies (Flyback vs. LLC)
- Evaluated efficiency, component stress, scalability, and cost
- Selected LLC resonant converter due to superior efficiency and soft-switching performance at higher loads

b) Flyback Converter Analysis

- Designed and tested Flyback converter in Continuous Conduction Mode
- Switching waveforms matched theoretical predictions, validating voltage gain and efficiency
- Built and assembled hardware prototype, including custom transformer with air gap for magnetizing inductance

c) LLC Resonant Converter Analysis

- Compared Half-Bridge and Full-Bridge LLC topologies; identified higher primary current and conduction losses in Half-Bridge configuration the Full-bridge was then selected
- Achieved Zero-Voltage Switching (ZVS) by operating in the inductive region
- Verified resonant tank behavior through simulation
- Prototype testing revealed gain degradation with increasing load, prompting redesign to include dominant parasitic effects
- Identified key challenges and proposed mitigation strategies for improved performance

d) Simulation and Modeling

- Developed detailed models for both converters across input range (6 V – 8.4 V)
- Simulations confirmed stable operation under light and heavy loads
- Validated theoretical calculations and supported design decisions

2. Hardware Design and Testing

a) Transformer and Component Design

- Designed custom transformer using PQ cores (3C90 ferrite material)
- Calculated turns ratio, air-gap spacing, and wire selection (Litz wire)
- Observed deviations between theoretical and measured inductance, informing iterative design improvements

b) LLC Converter Hardware Implementation

- Built and tested LLC resonant converter prototype
- Verified operation below and above resonance under light load conditions
- Identified impact of parasitics on real-world performance

c) PCB Design

- Implemented Full-Bridge LLC schematic design using FAN7688 controller
- Designed schematic of isolated gate driver circuits to drive full-bridge configuration
- Designed schematic Integrating resonant tank, secondary rectification and filter stage

3. Controller Development and System Integration

a) Control Implementation

- Used TI LaunchPad to generate open-loop PWM signals for both LLC and Flyback converters
- Successfully drove MOSFET switching in simulation and hardware setups
- Initiated closed-loop control development to regulate output voltage via frequency modulation

b) System Integration and Control Strategy

- Designed framework for feedback control: output sensing → error calculation → frequency adjustment
- Enabled foundation for adaptive control of resonant converter operation

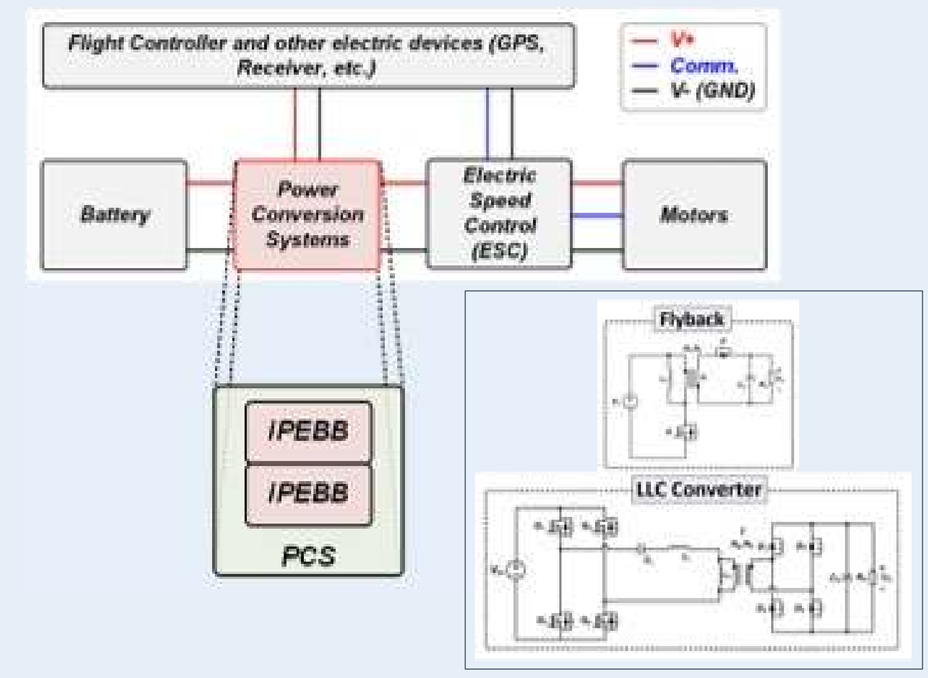
4. Drone System Integration and Troubleshooting

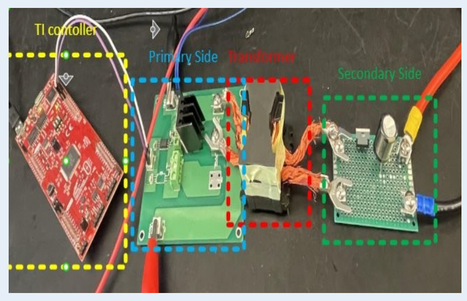
- Integrated full drone control system including transmitter, receiver, flight controller, ESCs, and motors
- Established reliable communication via IBUS protocol and validated signal integrity
- Verified ESC initialization and motor response to control inputs
- Achieved stable system operation, providing a validated platform for future power electronics integration

Project Outcome

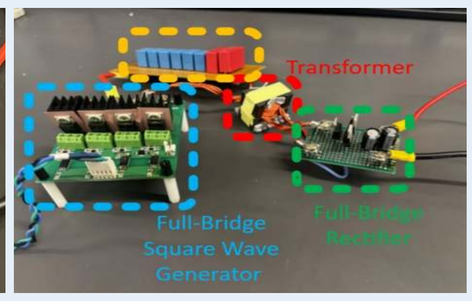
Unfortunately, our ABO was not achieved. The team encountered similar challenges as the previous group which slowed down our progress. These roadblocks were identified and solutions were proposed to mitigate the design challenges and fast track the progress of next year's teams.

Figures



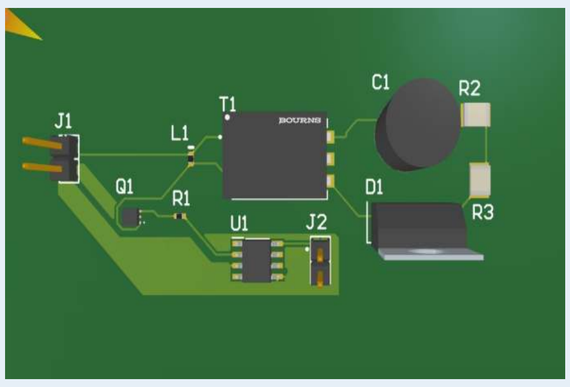


Flyback Converter Prototype



LLC Resonant Converter Prototype

Full-bridge LLC PCB Layout



Flyback PCB Layout

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Prober Error Tracking & Evaluation

Web tool to display error frequency and messages associated with in-house hardware.

Team Members: Robbie Stevens (CPE), Evan O'Neill (ELE)

Technical Directors: Alfred Binder, Liam Crisfield, & Josh Hoyle

Project Motivation

Vicor utilizes a variety of equipment to electrically test die on their silicon wafers that will be used in their assembled parts. One of these pieces of equipment that are used is called a prober. The probers are designed to test multiple wafers and run tests on all the die contained in each wafer. The process is extremely time consuming, and can run both occurs is that the probers covernight and into the weekend. Because of this, one problem thatan encounter errors that will pause the testing process. The process will remain halted until an operator can fix it. To tackle this problem, Vicor wants to know how often the probers stop during the testing process, and why the test had to be halted. With the information gathered from tracking the probers, Vicor will be able to accurately schedule maintenance for faulty equipment, and allocate personnel efficiently based on the data collected by the tool.

Key Accomplishments

Extraction of Key Files & Information: Each prober outputs three types of files: event, error and profile logs. By extracting and understanding the files being output by the prober, we were able to make critical decisions in our scripting to determining what points we will be able to show on our web tool, based on the display messages.

Parsing Additional Data: In addition to the data that was parsed in the previous iteration of our code, we added additional functions to parse new data that was provided to us. This data includes the ID number of the wafer, the Product ID, the REC number that tracks which events are occurring during the testing phase, as well as the cassette loading and completion times to track the overall time it took to test the wafer.

Correlation of Event & Error Logs: Across two of the logs, event and error, there are many instances where an event and error occurred in unison, and one message could explain when and why the other happened. By combining the results of correlated events and errors into one data point, our tool will be able to display this critical information to troubleshooters who can work efficiently to rectify the machine.

Updated Downtime Tracking: In the previous version of our parsing script, we calculated the downtime tracking of the probers based on the changes in state values that indicate when the prober pauses and then resumes its testing. With this new iteration, our script now tracks the values of the prober's alarm pole values to indicate when the prober stops and continues its testing. This provides a more precise time of when the testing states are changing, and when calculating the the downtime, provides us a more precise difference in the time between when the testing process initially pause and resumed its testing,

Database Implementation: With all the necessary data extracted, we then implemented a function that uploads the parsed data directly into a database hosted by Firebase. Because the extracted data was stored into several text files, we had to convert those into JSON files for easy transfer. Once the text to JSON function was was working, we then created our function that takes each JSON file and uploads them as individual documents into our database, as seen in **Fig. 2**. This allowed us to store all the data we pulled in a more organized format rather than just writing the pulled data into text files.

Downtime Visualization: With the data we collected, we then needed to implement our web tool that will allow the users accessing the data to see different trends in the data being collected. This is so the prober operators can better understand when and where certain errors may have occurred. This was accomplished through means of creating graphs based on the desired data the user wishes to view. In **Fig. 1**, we have an example of a graph showing the downtime that occurred throughout a single day of prober testing. Along the x-axis are the timestamps that indicating the starting time of a process first began prior to stopping when the prober encountered an error. Along the y-axis is the downtime seconds that were recorded when the process was paused and had to wait for a prober operator to resolve the error. As seen in the graph, many of the errors that were encountered were resolved fairly quickly, while one took an extremely long time to be fixed. Also visualized in **Fig. 3** is a second interface that showcases the exact times that one prober was down during an 8 hour period. Green in this view shows uptime, while the red shows every interval that the prober is not probing

Frequency Visualization: An important aspect of the web tool developed is to show how frequently different REC codes occur during testing. This allows prober operators to quickly identify which types of events or errors are happening most often, and potentially diagnose recurring issues in the testing process. As shown in Fig. 4, the interface displays the top REC codes on the x-axis and their corresponding frequency on the y-axis. By filtering the data based on time range, REC type, or specific dates, users can narrow down when certain events are most prevalent. This visualization helps highlight patterns, such as specific REC codes appearing more frequently during certain shifts or testing phases, allowing operators to make more informed decisions about maintenance, troubleshooting, or process improvements.

Anticipated Best Outcome

The Anticipated Best Outcome for this project is to research, design, and implement a fully functioning system that collects and displays information about these prober errors. The system will include collecting data recorded by the probers, data processing to organize and calculate the data as needed, database management to organize and store the data in an easily accessible way, and data access for users to be able interact with the data directly. When the system becomes fully operational, then data driven decisions can be made.

Project Outcome

The Project Outcome was to create a system to help better understand and prepare for prober errors. We met the anticipated outcome

Figures

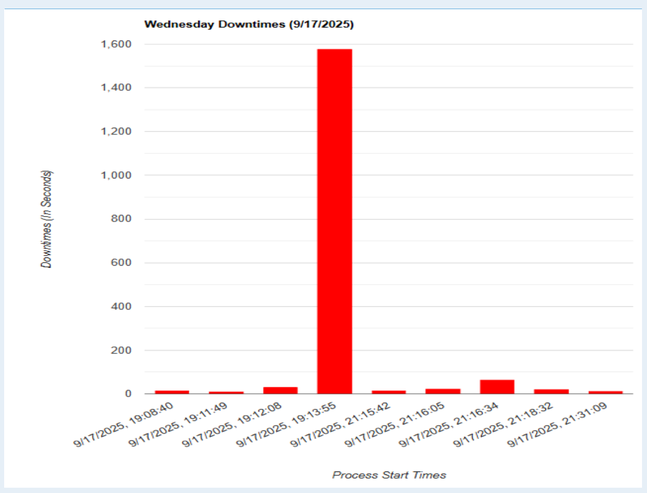

Fig. 1: Sample Graph Showing the Downtime Seconds From One Day of Prober Testing

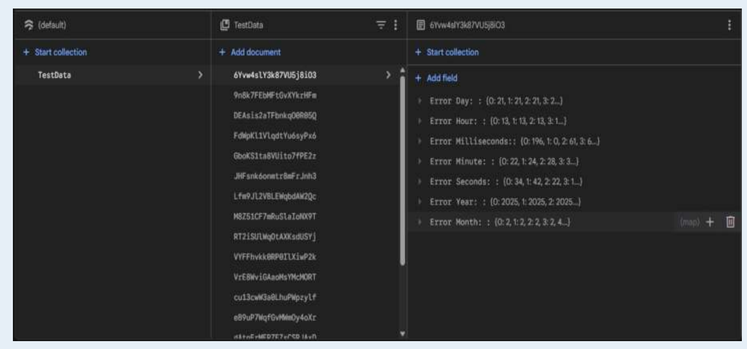

Fig. 2: Database Storing All The Data That Has Been Collected By Probers

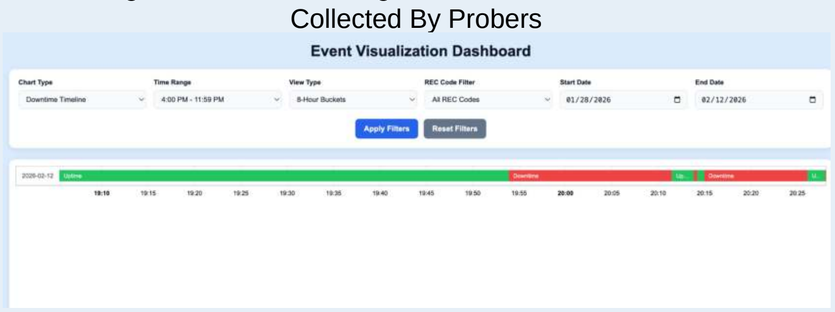

Fig 3: Web tool showing a timeline of uptime and downtime through the duration of an 8 hour period

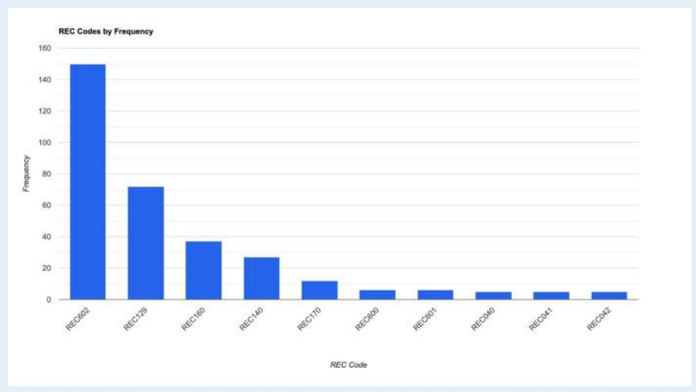

Fig 4: Sample Interface Showing the Frequency of Certain REC Codes in a given time period

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RMA/FSI Resource

RMA/FSI WORK INSTRUCTIONS

Team Members: Denilo Semedo (ELE)

Technical Director(s): David Paul, Liam Crisfield, Chris Couto

Project Motivation

Vicor's customers require failure analysis labs to examine excursion and outlier failing modules and components identified through Returned Material Authorization (RMA). These items undergo submission validation and may need Fail Site Isolation (FSI) before destructive processing to expose physical failure characteristics and determine corrective actions. This process varies based on failure types and product designs. As Design Engineering standardizes solutions, improved Failure Analysis success rates and reduced cycle times would enhance customer confidence in product quality and control.

This project focuses on developing a prototype curve trace solution for a controller in a cut-in module. The goal is to create and verify two work instructions for product ramp-up, ensuring RMA modules with new P07X and P08X integrated circuits can be: (1) validated through ATE and Unpowered Curve Trace Testing using Robson Technologies Inc., and (2) processed through Fail Site Isolation with Functional Bench Testing.

Anticipated Best Outcome

1. Develop clear **work instructions** for Electrical Analysis and Fail Site Isolation (FSI) of RMA failures.
2. Document procedures to preserve module packaging during **curve trace** and **ATE validation**, in collaboration with Test Engineering.
3. Include **backside bench techniques** for FSI and coordinate with Design Engineering on **failure-excitation methods** (thermal cameras, Scanning Optical Microscopy, programmed test modes).

Key Accomplishments

Electrical Analysis Research

- Completed in-depth study of electrical characterization methods used in semiconductor FA, including curve tracing, IV sweeps, and leakage/breakdown detection.
- Mapped abnormal electrical signatures to likely defect mechanisms and their role in Fail Site Isolation (FSI).

ATE Validation Process Review

- Analyzed Automated Test Equipment (ATE) validation flows, parametric limits, and correlation procedures.
- Established understanding of how electrical failures are screened, categorized, and routed toward RMA and FA.

Backside Fault Localization Methods

- Researched backside analytical approaches such as silicon thinning, IR techniques, and laser-based excitation.
- Identified scenarios where backside access improves localization of buried or inaccessible defects.

Documentation Standards

- Reviewed internal documentation expectations, including revision control, formatting, and work instruction structure.
- Ensured future deliverables align with professional engineering standards.

FSI Tools & Fault Localization Techniques

- Studied operational principles and best-use cases for tools such as SOM, Thermal Imaging, and Emission Microscopy.
- Compared contrast mechanisms and excitation strategies to determine ideal methods for specific failure signatures.

Hardware Development

- Selected and validated appropriate pogo pins for test reliability.
- Designed and developed a custom daughter board to support FA and FSI testing.

3D Socket Design

- Initiated design of a **custom 3D-printed IC socket** to enable rapid device insertion and electrical probing.
- Developed preliminary mechanical alignment concepts to improve repeatability during testing and fault localization.
- Evaluated socket geometry requirements for accessibility during electrical characterization and backside analysis.

Project Outcome

While the anticipated final outcome was not fully realized, roughly 40% of the intended work was completed, providing critical groundwork and technical understanding to support future continuation of the project.

Figures

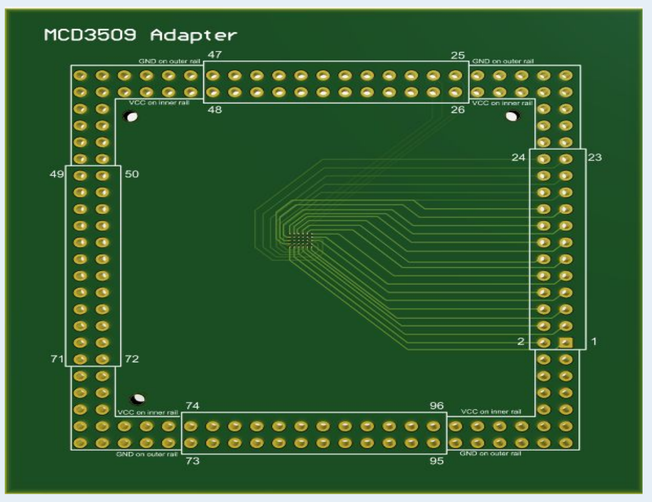

Figure 1: Designed Daughter Board

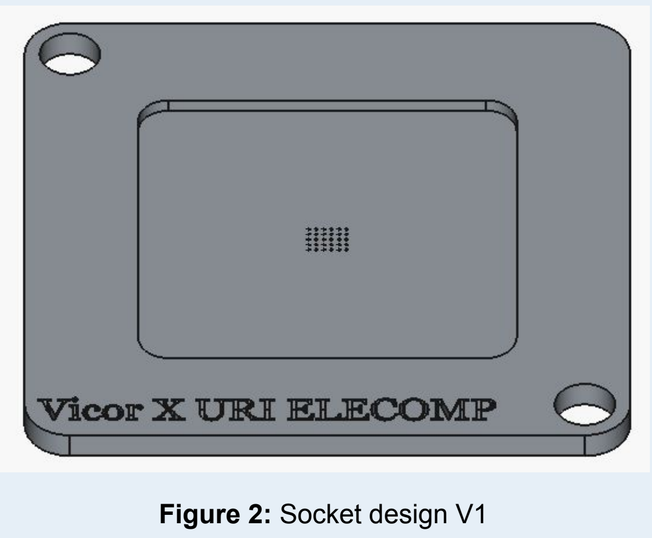

Figure 2: Socket design V1

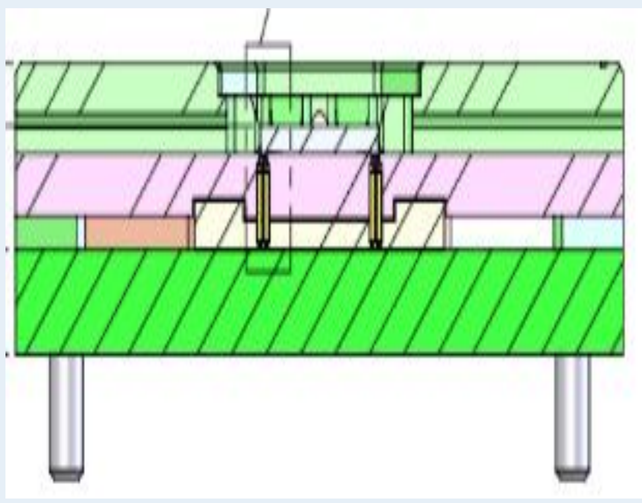

Figure 3: Stackup of PCB and probes

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VoltServer: CLEAR

LED Sequential Communication Protocol Application

Team Members: Joshua Pereira (CPE), Ryan Tattrie (ELE)

Technical Director(s): Camilo Giraldo, Chris Rothwell(CTD)

Project Motivation

The status codes for each VoltServer device are different but follow the same general style of light-blinking sequences. Currently, VoltServer engineers must manually decipher these codes, which involves looking them up and watching the sequence repeat multiple times. This process is inefficient, slows down troubleshooting, and can be troublesome for both engineers and technicians working in the field. As VoltServer systems expand, relying on manual interpretation becomes even less practical. The VoltServer Clear project aims to address this issue by developing a cross-platform application capable of recording and automatically decoding these blink patterns through a mobile device's camera. By streamlining interpretation and reducing dependence on documentation, the application can significantly improve diagnostic speed and accuracy. In addition, because the codes will be scanned digitally, there is an opportunity to embed real data within high-frequency LED blinks, expanding the usefulness of existing status indicators and enabling more robust device communication.

Anticipated Best Outcome

The Anticipated Best Outcome for the VoltServer Clear project is a proof-of-concept cell phone application that can use the camera to scan blinking LEDs on a VoltServer device and determine what the LED code is telling the user. There will also be a blink code test board with embedded microprocessors, sensors, and LEDs that will be used to simulate the LED codes. The best outcome consists of both the cellphone application and the blink code test board working together to demonstrate the feasibility of embedding data through the LEDs

Key Accomplishments

PCB Test Board Schematic and Layout:

During the design process of the schematic, we researched various parts that accomplished the tasks we needed the board to accomplish. We had to switch out the microcontroller near the end of the design process to alleviate the need of having a bluetooth connection with the app to control what tests are being blinked. That was the only obstacle we faced pending any size issues with certain components such as resistors and capacitors, but initial looks at the sizes seem to point towards everything working as intended. We were able to review the final design schematic and move on to the next step. We then were able to create the layout for the PCB

Ordered Blink Test Board:

After finalizing the layout, we ordered five LED Blink Test Boards through JLCPCB. After the first order, we were informed that the footprints we provided did not line up with the corresponding parts we had to sub out. We subsequently redesigned the layout and resubmitted the order, which was accepted and promptly manufactured and delivered within a week. **(Fig. 1)**

Flutter Camera Application and Cloud Pipeline:

During development, we evaluated several Flutter camera packages and selected the video_player library for its stability, ease of integration, and strong community support. Using this library, we built a prototype app **(Fig. 2)** that allows users to record a video or select one from their device's media library, preview it in-app, and upload it directly to Firebase Cloud Storage. Once uploaded, the file triggers an Eventarc event, which invokes a containerized Cloud Run service to execute the OpenCV processing pipeline. The backend handles event parsing, downloads the video, and coordinates processing before storing structured results in Cloud Firestore for frontend retrieval. The frontend integrates Firestore listeners to dynamically display processed results within the application **(Fig. 4)**.

OpenCV Processing:

To process LED blink patterns, we selected OpenCV for its strong support for frame-level video analysis and Python workflows. The backend is modularized into three components: main.py (orchestration), video_processing.py (signal extraction), and sequence_matcher.py (classification). The main.py entrypoint handles event parsing, video retrieval, and coordination of the processing pipeline. The video_processing module analyzes the video frame-by-frame, extracting frame rate information and converting frames from BGR to HSV color space to isolate red, green, and blue LED signals using tuned thresholds. Morphological filtering is applied to reduce noise, after which binary sequences are generated per channel and converted into time-based on/off representations. The sequence_matcher module then normalizes and compares these sequences against predefined LED blink patterns using Dynamic Time Warping **(Fig. 3)**, enabling accurate classification despite timing variation. Channel-aware validation is applied to reject inconsistent matches, producing a final detected state and confidence score that are stored in Firestore for frontend retrieval.

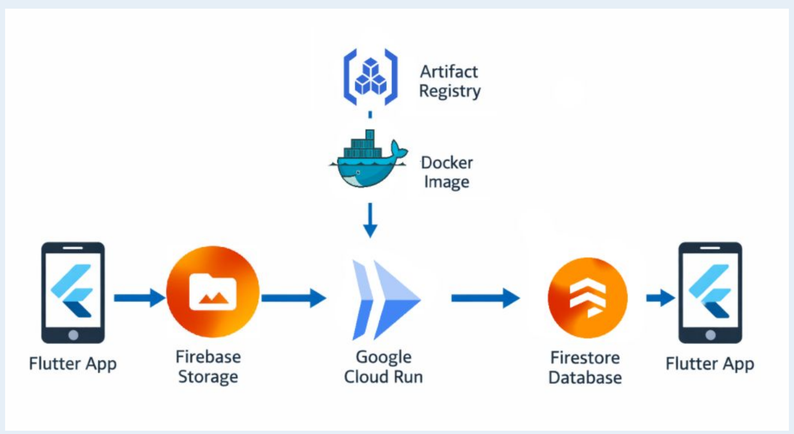

Fig. 4: Cloud Pipeline

Project Outcome

We did not achieve the Anticipated Best Outcome. VoltServer was provided with a working LED Blink Code Detection app, but was not delivered a working Blink Test Board, which also resulted in no bluetooth capability.

Figures

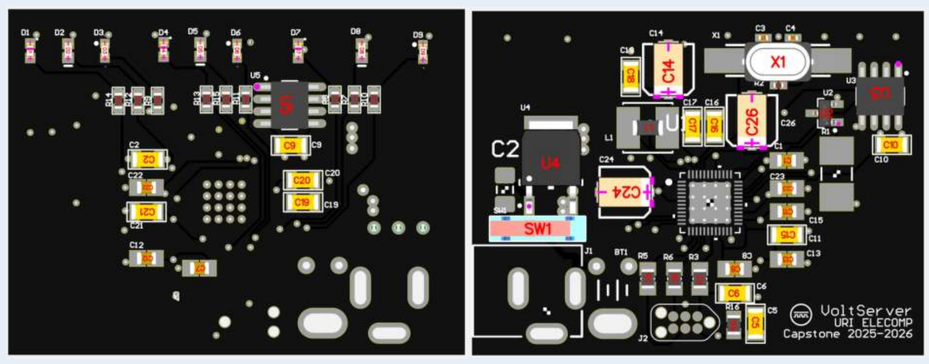

Fig. 1: The layout of the PCB Test Board

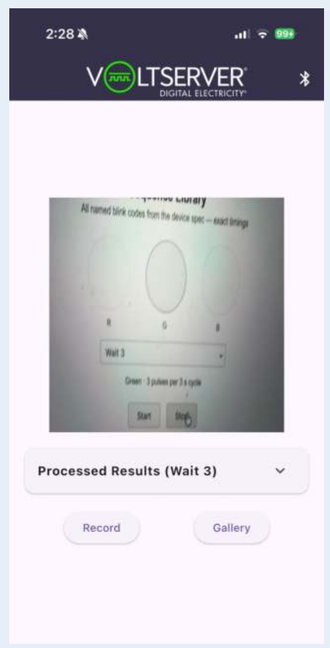

Fig. 2: The Flutter App UI

```python
def dtw_distance(a: list[float], b: list[float]) -> float:
    n, m = len(a), len(b)
    if n == 0 and m == 0:
        return 0.0
    if n == 0 or m == 0:
        return math.inf

    dp = [[math.inf] * (m + 1) for _ in range(n + 1)]
    dp[0][0] = 0.0

    for i in range(1, n + 1):
        for j in range(1, m + 1):
            cost = (a[i - 1] - b[j - 1]) ** 2
            dp[i][j] = cost + min(dp[i - 1][j], dp[i][j - 1], dp[i - 1][j - 1])

    return math.sqrt(dp[n][m])
```

Fig. 3: Dynamic Time Warping Algorithm

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XMOS - XNAV

Realtime Robotic Control on xcore.ai

XMOS

Team Members: Aidan Donnellan (CPE), Zachary Weinstein (CPE|ELE), Emily Katz (ELE|GER)

Technical Director(s): Dr. Andrew Cavanaugh and Chris Rothwell (CTD)

Project Motivation

A mobile robot is the perfect platform to demonstrate some of the key benefits of xcore.ai chip: precise IO control, high performance processing cores, and software defined communication interfaces. Of these interfaces will include one linking the xcore.ai chip and the roomba, one linking the chip and the wireless transceiver, and the last linking the chip to additional sensors. Robotics demands tight synchronization between sensors and actuators. xcore.ai's hardware level deterministic timing and multi-threaded I/O enable reliable, low-latency handling of encoders, motor drivers, ultrasonic sensors, and more without relying on external peripherals or interrupt-heavy MCU code. The parallel architecture and real-time scheduling of xcore.ai allow it to run closed-loop motor control, sensor fusion algorithms (e.g., IMU + odometry), and obstacle avoidance logic concurrently, on a single chip. This demonstrates how the xcore.ai chip can handle complex, time sensitive workloads typically spread across multiple components (XMOS).

Anticipated Best Outcome

The anticipated best outcome of this project would be to show off the capabilities of the XMOS xcore.ai chip in a real-world robotics context. In doing this it would be showcasing the unique capabilities in deterministic real-time control, parallel processing, and low-latency I/O. Proving the performance and reliability of this application through this project helps XMOS' strategic goal of expanding into the robotics, industrial automation, and intelligent edge systems markets. Beyond this we may combine ABOs with our sister team XROS. This would combine our ABO with theirs of creating a micro-ROS server furthering our main goal of proving the xcore viable for robotics.

Key Accomplishments

Robot Platform Selection (Roomba 600 series): The team went through a few different options for prebuilt platforms that would be best for the project. The Roomba platform was chosen over others for a couple reasons. Roomba 600 series has support to connect with any external microcontroller through the Roomba Open Interface and is highly documented. The prebuilt comes with almost all sensors we need out of the box, and the platform is the cheapest by far compared to other platforms we looked at.

System Architecture Design: The initial system architecture has been defined and documented. The Block Diagram **(Fig. 1)** outlines the interactions between the xcore.ai processor, built-in and external sensors and telemetry. Through this diagram we have planned out how we intend to reach our anticipated best outcome through this system design. The diagram is robust but also will be easy for us to modify as we learn more about the hidden challenges that come with any technical project.

External Sensor Integration: The roomba prebuilt system might have all we needed to reach our best anticipated outcome. However, adding extra external sensors like a camera **(Fig. 1)** made the system more robust and improved our ability to show off the parallel capabilities of the xcore.ai processor. The camera will allow for better navigation through computer vision helped with maintaining a consistent pathing throughout the course proving robustness.

Machine Learning Application: Machine learning is used in computer vision navigation systems on the robot. This could have been developed in a number of different ways. We had considered if this model would be on the robot itself or done server side and transmitted. As we discussed options with our technical directors we started to create a list of many different machine learning applications beyond computer vision and created a diagram of use cases **(Fig. 2).** We decided to go with an onboard model talking directly with the camera. Some of our initial tests included converting camera data into ascii images representing a frame taken by the camera **(Fig. 3).** Testing was also performed on a mock setup of the robot using a Raspberry Pi, running the machine learning model and receiving instructions for commands **(Fig.4).**

Telemetry and Data Stream Setup: we added wireless transceiver to the robot system in order to wirelessly track telemetry **(Fig. 1)**. Having some type of telemetry is part of the requirements for our anticipated best outcome. We will also had options for wired telemetry as a fallback onboard the robot system. Having this transceiver also opens up opportunities for remote control and off board machine learning applications. We can host the model server side and transmit the commands **(Fig. 2)**.

Autonomous Navigation : One of the main objectives of the XNAV project is to create an autonomously navigating robot. Specifically a robot capable at the very least of following a set path and can respond to outside stimulus without user input. The stimulus in the form of bump detection, path following through computer vision.

Testing Course: Setting up and deciding how the robot will autonomously navigate went hand in hand with how we designed the testing course. The testing course is how we present the final product and as proof of us completing our best anticipated outcome. The basic idea is to set a course the robot has to follow.

Project Outcome

We were able to meet the anticipated best outcome. XMOS was given a full report on the project and our findings that they could potentially use in the future.

Figures

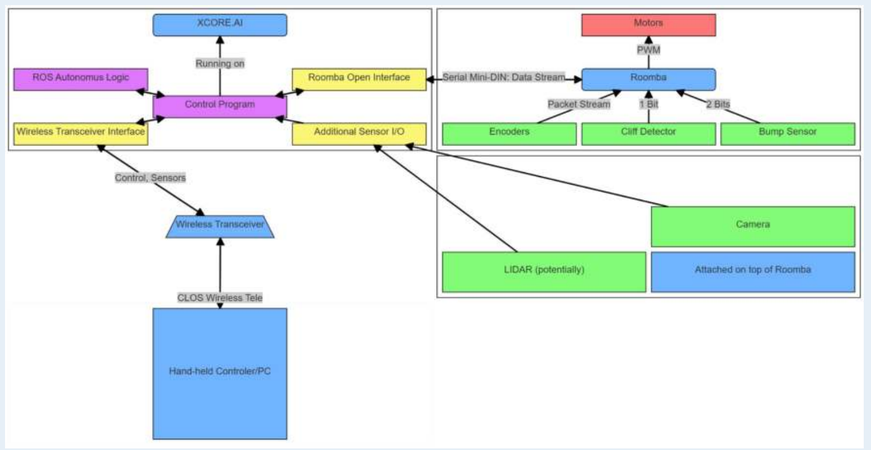

Fig. 1: *Block Diagram of System Architecture*

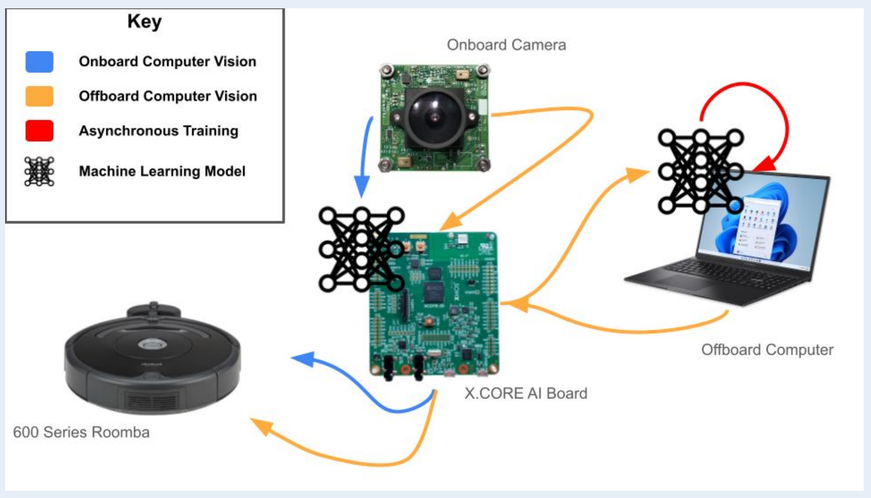

Fig. 2: *Machine Learning Application Diagram*

Fig. 3: *Camera Ascii Image Testing*

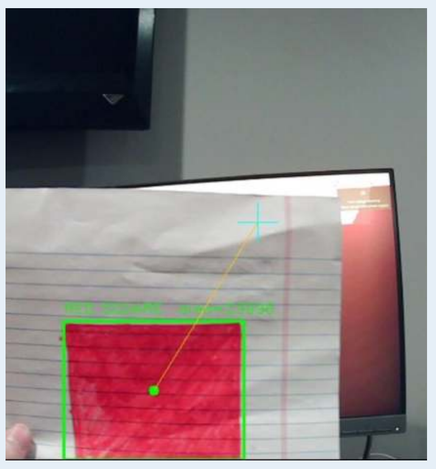

Fig. 4: *Mock Machine Learning Program*

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Porting Micro ROS to xcore.ai

XMOS

Team Members: Abigail Tadamala (ELE), Jacob Mathews (CPE), Lyneth Mendoza (CPE & ELE)

Technical Director(s): Andrew Cavanaugh

Project Motivation

Robotics applications increasingly depend on standardized middleware like ROS 2 to support modular development, real-time data sharing, and system interoperability. Although ROS 2 is widely used in research and industry, its adoption in resource-constrained, real-time embedded environments remains limited. The project will attempt to address this challenge by extending ROS 2 concepts to microcontrollers, support for the XMOS xcore.ai platform, a highly parallel, deterministic, and software-defined embedded processor is currently missing.

This project aims to close that gap by bringing micro-ROS to xcore.ai, demonstrating how a modern embedded architecture can operate as an efficient, reliable ROS 2 compatible node. With its unique combination of parallel compute, deterministic I/O, and low-latency execution, xcore.ai is particularly well-suited to robotics and time-critical control applications. Enabling micro-ROS on this platform not only broadens its applicability within distributed robotic systems but also reduces dependence on external communication processors and highlights XMOS technology within an industry-standard robotics ecosystem.

Anticipated Best Outcome

The best outcome is :

- Running micro-ROS node on XMOS xcore.ai publishing/subscribing to a ROS 2 network. This network should include a node running ROS 2 on a Raspberry Pi and connect to the xcore.ai using CANBUS.
- Benchmark round-trip latency and jitter.
- Example integration with a robot or simulation
- Integrate with XNAV project and create a production release

Key Accomplishments

A major accomplishment of our project has been developing a functional ROS 2 server capable of bridging communication between the xcore.ai platform and external micro-ROS nodes (**Figure 1**). We designed the core server architecture, integrated it into our development environment, and ensured seamless interaction with the XTC Tools and XMOS SDK. We successfully validated this system by testing it against an ESP32 running micro-ROS, confirming stable topic publishing, subscribing, and message integrity over serial communication. Alongside this, we established the project's system design, researched ROS 2 image compatibility across various platforms, set up our Raspberry Pi development host, and created a clean, maintainable repository and developer workflow to support ongoing development.

A second major accomplishment has been successfully flashing a basic version of FreeRTOS onto the xcore.ai. This provides the foundation for running our micro-ROS node natively on the platform. The FreeRTOS build currently reads IMU data, essential I/O functionality which will be necessary for future RTOS-based development. In addition, we determined the tile mapping for optimal utilization of the xcore.ai (**Figure 2**), dedicating the majority of the logical cores to the FreeRTOS with microROS node and reserving two cores for required drivers and tile interconnect. This mapping will guide our resource allocation strategy as we scale up the complexity of our application.

A third major accomplishment has been establishing the micro-ROS test environment. We have procured and begun configuring the Hiwonder MentorPi A1 Robot Car (**Figure 4**), a ROS2-based autonomous robotics platform equipped with lidar, depth sensing, and onboard AI capabilities. This system provides a robust foundation for real-world testing of autonomous navigation, perception, and control. Our next step is to transition the platform from its default Raspberry Pi architecture to the xcore.ai hardware. This involves rewiring and reconfiguring the system to support micro-ROS nodes running directly on xcore.ai, enabling real-time performance validation and tighter integration with embedded systems. Once complete, this platform will allow us to evaluate micro-ROS node performance in a realistic autonomous driving environment. It also shows that we could integrate with the XNAV project to go beyond the ABO stage.

A fourth major accomplishment has been improving the overall xcore.ai development workflow to make the platform easier to configure, build, and maintain. We updated the Docker environment to include the XMOS toolchain, XTC tools, and prebuilt micro-ROS dependencies directly within the image, creating a more portable and self-contained development setup. We also added wrapper scripts and entrypoints to streamline environment setup and automate common tasks such as container startup, firmware configuration, building, flashing, and agent launch. In addition, we created reference documentation and integration checklists to support future development and provide a clearer path for extending the xcore.ai micro-ROS platform as the project continues.

A fifth major accomplishment has been successfully porting the Micro XRCE Client onto the XMOS SDK, enabling native micro-ROS communication on the xcore.ai. This required adapting the client to the XMOS architecture and implementing a custom transport layer to interface with the FreeRTOS based UART communication protocol used by the xcore.ai.(**Figure 3**) The client now successfully compiles and runs on the xcore.ai, making a critical milestone in achieving a full micro-ROS stack integration on the hardware.

Project Outcome

The project has made significant progress toward the anticipated outcome. We successfully built and deployed the micro-ROS firmware onto the xcore.ai platform and established a functional FreeRTOS foundation for embedded operation. While full communication between the ROS 2 server and the xcore.ai micro-ROS node is still being finalized, current efforts are focused on resolving integration challenges to achieve stable data exchange.

Figures

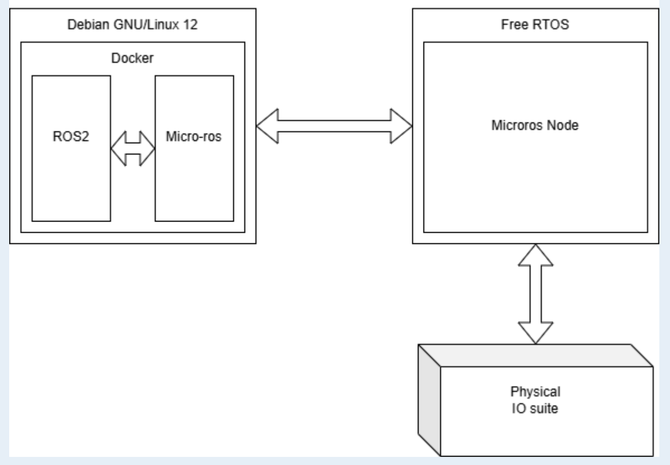

Figure 1 - High Level Project Overview

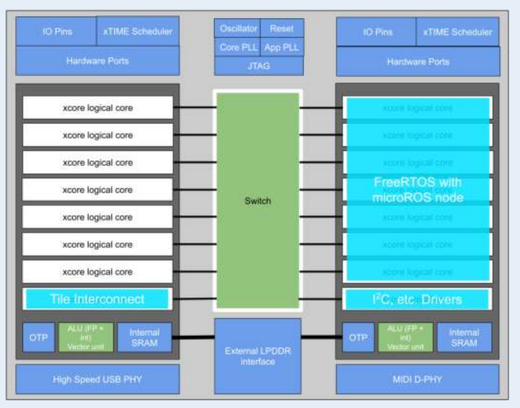

Figure 2 - xcore.ai Tile Mapping

Figure 3 - micro-ROS Set Up

Figure 4 - HiWonder MentorPi A1 Robot

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Zebra AI / ML

Empowering Printer Calibration with Object Recognition & Analysis

Team Members: Richard Buckley (CPE), Sergio Herrera (CPE), Jacob Silva (CPE)

Technical Director(s): Matthew Corvese, Patrick Hegarty

Project Motivation

Thermal label printers are expected to deliver consistent, high-quality output across a wide range of label stocks, including many low-cost third party media. Large enterprises (e.g., Amazon, FedEx, USPS) aggressively pursue cost savings, and small differences in media pricing add up at scale. However, every change in media chemistry or supplier can alter print behavior, affecting dot gain, bleed, and overall readability. Today, Zebra engineers spend significant time manually tuning printer parameters, responding to customer requests to make a new media type "print correctly". By introducing AI-driven analysis of printed patterns, Zebra can automatically detect print defects and recommend or apply optimal settings. This reduces manual calibration work, shortening deployment time for new media; allowing engineers to focus on higher-value design and innovation.

Anticipated Best Outcome

The best outcome for this project is:

- Develop and train a machine learning model that:
  - Identifies printed patterns and objects on printing labels
  - Compares them to an “ideal” reference
  - Automatically adjusts print parameters to achieve optimal printing quality

Key Accomplishments

Custom Python Driver & Raspberry Pi 5 Setup: To enable bidirectional communication between the Raspberry Pi 5 and Zebra printer **(Fig. 1)**, we developed a custom Python-based USB driver that overcomes the limitations of proprietary or one-directional solutions. Our system utilizes the 64-bit Raspberry Pi OS, featuring a unified environment accessible via SSH and VS Code tunnels. This setup ensures seamless remote code execution and full reproducibility for all project collaborators.

Test Pattern Label Design: We had a few different iterations but eventually settled on a pattern that printed only a single row of test patterns. Though this may seem wasteful, we struggled to create any reproducibility in our data with multiple rows, as it introduced too much variability in the hidden state of the system.

Print-Capture-Validate Loop: To actually collect our data, we needed an automated approach that allowed us to efficiently print the test pattern, knowing when THAT test pattern was in view of the camera (the distance between where the paper is fed out of the printer and the camera is ~400 dot lines), and then ensuring that we are not mixing up different types of data **(Fig. 2)**.

Segmentation Pipeline: Our original segmentation approach relied on detecting L-shaped corner markers to warp and standardize the label image. This method failed entirely on blank or low-ink labels. We redesigned the pipeline to use a known expected template as a geometric reference. The system parses the template to locate all 27 cross symbol centers, clusters them into a grid, and uses an affine transform to align the grid to the actual label capture, making segmentation robust even when the label has little to no visible ink.

Synthetic Label Pipeline & YOLO Retraining: When switching to single-row continuous printing broke our existing YOLO detection model, we built a synthetic label generation pipeline to produce malformed label examples at scale. This data was used to retrain YOLO on URI's Unity L40S GPU cluster, restoring robust detection across all print conditions.

Ranking-Based Training Approach: After finding that absolute scoring did not yield a normal distribution across print conditions, we pivoted to a ranking-based model. Human-in-the-loop fine-tuning was implemented via a Streamlit app that allows operators to rank printed dot patterns relative to each other, generating a rich labeled dataset without requiring absolute ground truth scores **(Fig. 3)**.

Attention-Based Final Model: We settled on an attention-based classifier using 5-channel input (incorporating data from 2 neighboring dot patterns). The model achieved 96.2% validation accuracy with correct generalization with consistent conditions reaching our Anticipated Best Outcome (ABO) **(Fig. 4)**.

Project Outcome

We met our Anticipated Best Outcome. Our final attention-based model achieves 96.2% validation accuracy in classifying dot pattern print quality from Zebra label printers, using a 5-channel input across 2 neighboring patterns. The full pipeline, from automated printing and camera capture, through segmentation, scoring, ranking, and model training, is complete and fully documented.

Figures

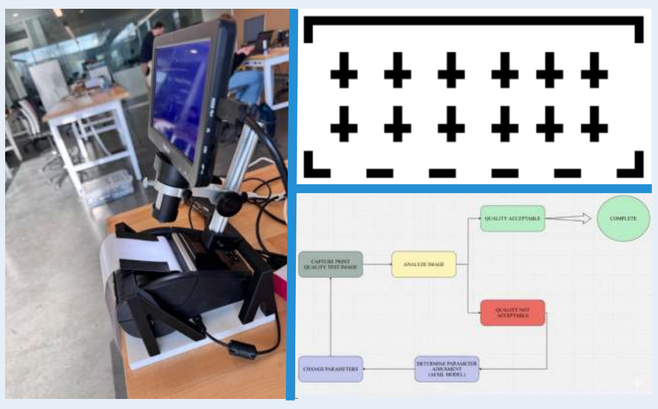

Fig. 1 & 2: Figure illustrating the experimental setup (left), the print–capture–validate workflow (bottom right), and the fiducial marker pattern used throughout the project (top right).

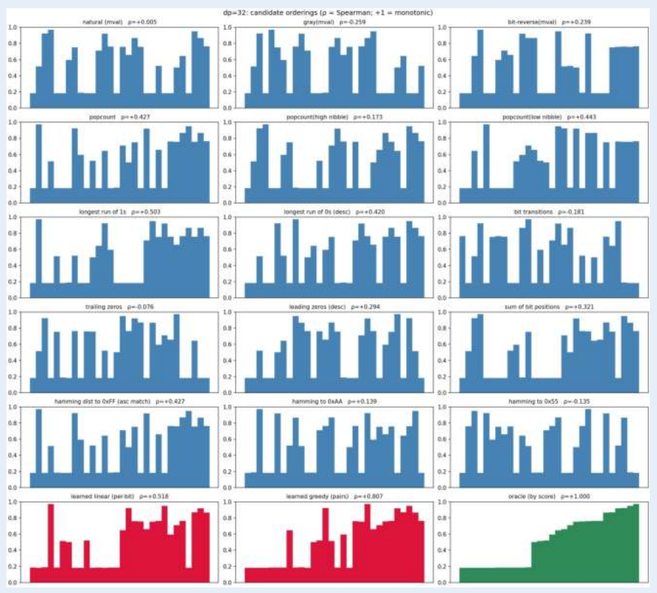

Fig. 3: Score distributions across candidate-ordering methods, illustrating a difficult regression problem: scores are clustered, irregular, and only weakly ordered.

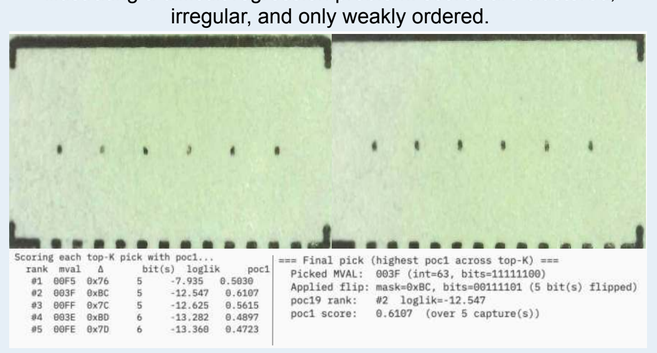

Fig. 4: Before-and-after example of the model’s recommendation: the input image is shown on the left, and the model-generated recommendation on the right.

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Peltier-Based Thermal Control System

Team Members: Jimmy Prior(ELE/CPE), Racquel Raphael(ELE), William Lucas(ELE)

Technical Directors: Anthony Helberg, Patrick Hegarty, Matthew Corvese; CTD: Mike Smith

Project Motivation

Thermal management plays a critical role in the performance and reliability of Zebra Technologies' industrial printers. During high-speed or continuous operation, uneven temperature distribution across the printhead can cause print quality issues, increased wear, and potential component failure. Existing systems rely on passive or limited control methods that cannot dynamically respond to changing thermal loads. This project was motivated by the need to develop a smarter, more responsive thermal control solution capable of maintaining consistent printhead temperatures under varying conditions. By integrating Peltier coils, a microcontroller, and the printhead's internal thermistor circuit into a closed-loop hardware control system, the team aims to enhance temperature stability, improve energy efficiency, and extend the operational life of Zebra's printing hardware. Beyond addressing these technical goals, the project also provides valuable hands-on experience in different electrical engineering–related fields such as embedded and control systems, preparing the team for future work in real-world engineering environments.

Key Accomplishments

Implementation of Closed-Loop Control System:
For the primary control element of the system, the Arduino Uno was selected for testing purposes and was ultimately used in the final prototype (**Fig. 3**). The microcontroller was programmed to utilize its Analog-to-Digital Converter (ADC) pins to obtain temperature readings from the printhead. This temperature reading provides the feedback signal for the closed-loop control system. Based on this input, the microcontroller outputs control signals used to regulate system operation.

Bidirectional Heating and Cooling Using Peltier Coils:
The thermal system consists of Peltier coils, heatsinks, and fans, which together allow for temperature regulation of the printhead(**Fig.4**). The Peltier coils function as the primary heating and cooling elements through bi-directional current flow. Heatsinks and fans are used to dissipate heat from the system and support thermal stability during operation .The overall system is driven by the microcontroller, which coordinates activation of these components based on feedback from the control loop(**Fig. 1**).

Power System Integration:
Two relay modules containing four relays in total were implemented to control the direction of current through the Peltier coils, enabling both heating and cooling functionality. They were also used to switch the fans on and off. The system was integrated with an Arduino Uno, which powered the relay modules for control. The fans and Peltier coils were supplied by external power sources, with the relays used to switch and regulate the applied voltage.

Data-Logging System:
We developed a controlled testing setup to evaluate the cooling system's effectiveness under real printing conditions. Using Arduino IDE for temperature data acquisition and a Python script for logging and visualization, we continuously track the printhead temperature while marking when printing starts and stops(**Fig. 2**). This allows us to directly compare thermal performance across different print durations and label quantities, identify performance gaps, and guide future design improvements.

Testing Procedures:
With data logging enabled through Python–Arduino integration using PySerial, we were able to evaluate the efficiency and effectiveness of the testing setup. Performance was assessed using benchmarks that measured how well the Peltier coils responded to heating and cooling demands. This analysis also included comparisons across different print conditions, with ink coverage ranging from 25% to 100% per printed label, to observe how changes in temperature affected system performance. In this context, temperature refers to whether the printhead becomes too hot during printing or too cold and requires preheating before printing.

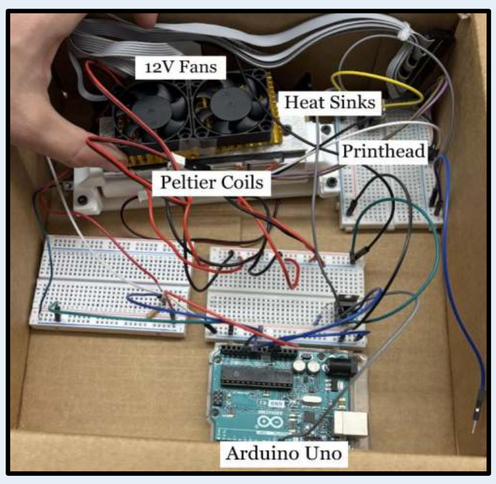

Fig. 4: *Initial Prototype of Control System*

Anticipated Best Outcome

Temperature Regulation: Maintains precise control of the printhead temperature within a defined range.
Hardware-Based Compensation: Performs temperature compensation via a dedicated hardware control loop.
Integration: Interfaces seamlessly with the printer system for real-time operation.
Data-Logging: Logs temperature data over time for diagnostics and performance analysis.
Modularity: Features a scalable and modular design for future upgrades or adaptations.

Project Outcome

The team was able to meet all outcomes except for implementing a modular design. In terms of improvement, the temperature regulation could be modified to enhance the efficiency of the cooling aspect of the system.

Figures

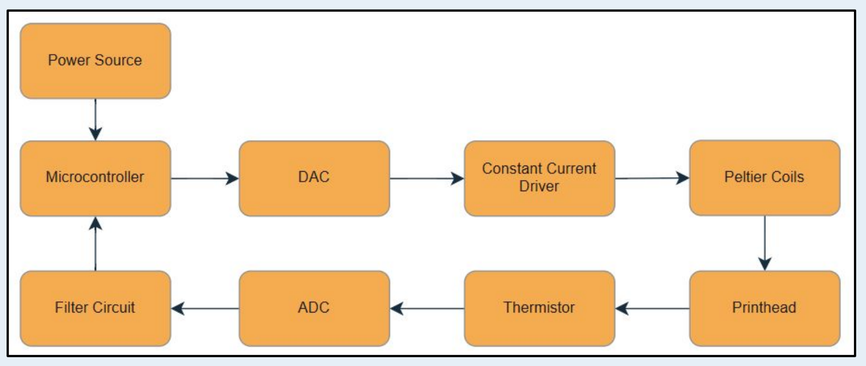

Fig. 1: *High-Level Block Diagram of Control System*

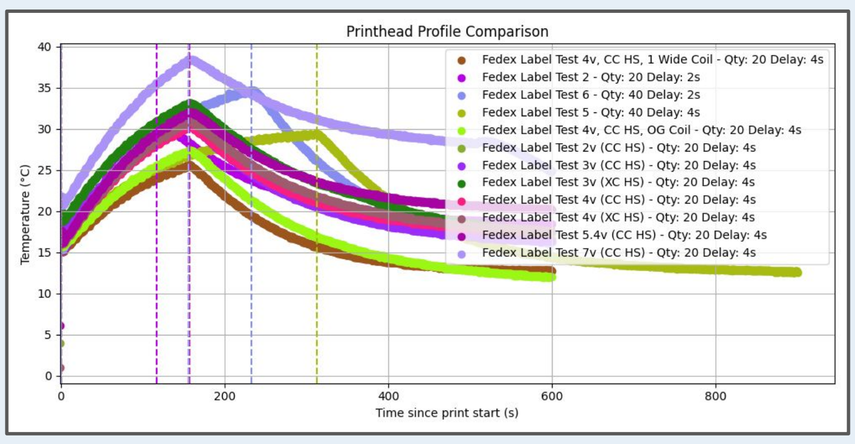

Fig. 2: *Data-Logging System with PySerial*

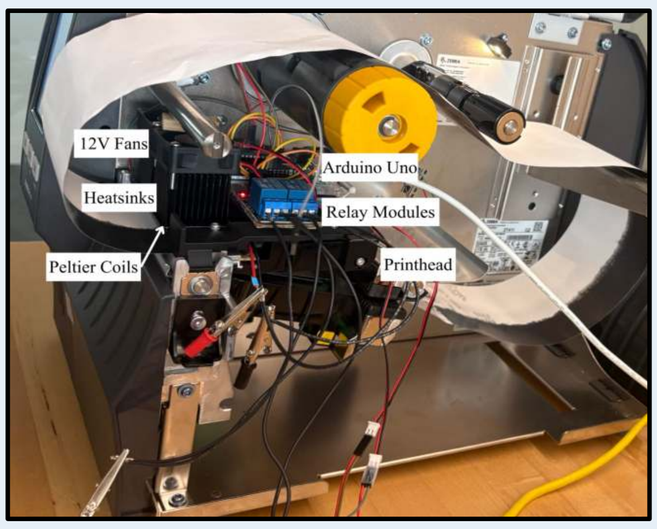

Fig. 3: *Finalized Prototype of Control System*

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Zebra - Resonance

On-metal RFID

Team Members: Nathan Vierkant (ELE), Destiny Moua (ELE), David Rodov (ELE)

Technical Director(s): Joseph Moreira, Eric Liberato; CTD: Mike Smith

Project Motivation

This project is focused on evaluating the feasibility of manufacturing on-metal RFID tags at Zebra. A key objective is to investigate a variety of antenna designs and analyze how their geometries and tuning techniques perform when placed on metallic surfaces. In addition to identifying designs that maintain strong read range and reliability in challenging environments, the project aims to expand the team's overall knowledge and understanding of RFID behavior on metal. Through systematic testing and analysis, we seek to develop optimized tag structures specifically suited for metal applications. Gaining insight into materials, design strategies, and production methods will also support an assessment of whether in-house manufacturing is a practical and cost-effective direction for Zebra. This effort is intended to establish a strong technical foundation that enables improved performance, greater customization, and more informed decision making for future RFID tag development

Anticipated Best Outcome

Achieve a clear and measurable improvement in the read range of a UHF passive on-metal RFID tag across both FCC and ETSI frequency bands, and create a tag that could be read on-metal from at least 6 meters away using Zebra equipment.

Key Accomplishments

AMC:

A perfect metal conductor (PMC) is some kind of material that blocks all magnetic fields. An artificial magnetic conductor (AMC) is a type of PMC though it is not actually 'perfect'. When an incident wave hits the surface of an AMC, the reflected wave is IN-PHASE with the incident wave. This is in contrast to a perfect electric conductor (PEC) which causes reflected waves to be out of phase by 180 degrees. An AMC typically consists of many resonators. In the case of our best performing tag, the resonators are small hexagons. The AMC tags we designed had two ground planes, one AMC, and a resonator patch. The tag was designed to be folded over two pieces of foam creating a three-layer tag. Various facets of the tag was adjusted to optimize read range. These parts include: resonator shape, resonator size, tag size, additional ground planes, stub thickness, and radiating patch angle.

Capacitive Gaps:

The capacitive gaps RFID tag design was developed to enhance impedance matching and current distribution for improved performance, particularly in on-metal environments. This approach utilizes strategically placing capacitive gap structures–typically in the form of closely spaced conductive fingers–to help introduce additional capacitance into the antenna geometry.

- Incorporated Artificial Magnetic Conductor (AMC) like structures to improve performance on metal surfaces.
- Implemented an Interdigital Capacitor (IDC) design to enhance impedance tuning and maintain efficient energy transfer.
- Achieved a measured read range of 2.08 meters in lab testing on metal surface.

Meandered Folded Dipole:

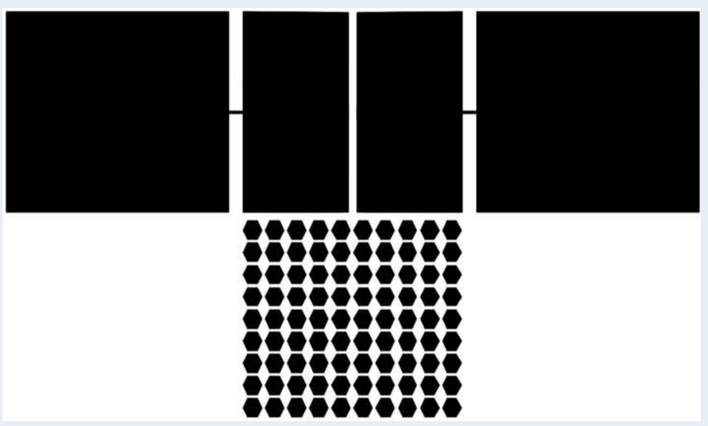
The antenna is a meandered dipole with an outer gain loop on a PET/foam substrate, sized at 101.86 mm × 33.95 mm using aluminum ribbon conductor, conjugate-matched to the NXP UCODE 8 IC at ~915 MHz. The CST surface current distribution (green antenna, arrows indicating current) is shown below, with current concentrating along the meandered arms and outer loop.

- 1 mm foam spacer isolates antenna from ground plane, direct contact severely degraded read range
- Measured on-metal read range: 2.3 m
- CST simulations inconsistent with physical results; measured performance is the primary benchmark

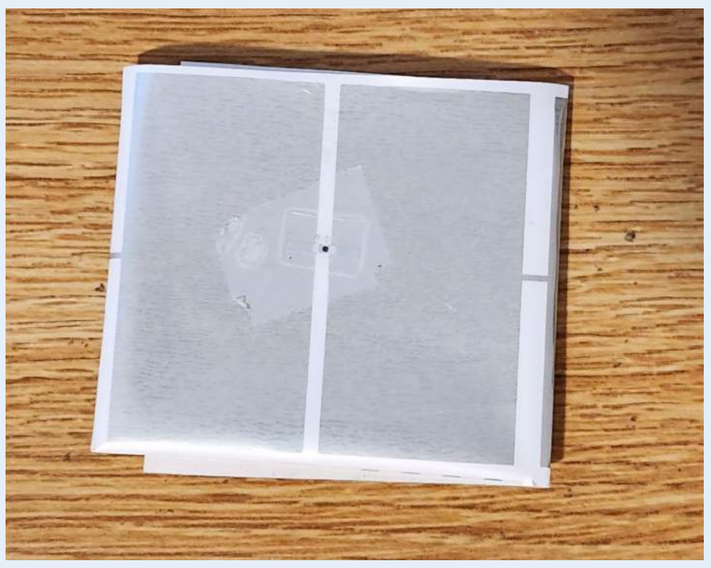
Project Outcome

Final design had a read range of 8.91 meters on-metal. Our project ended up focusing on only the FCC standard due to equipment restraints.

Figures

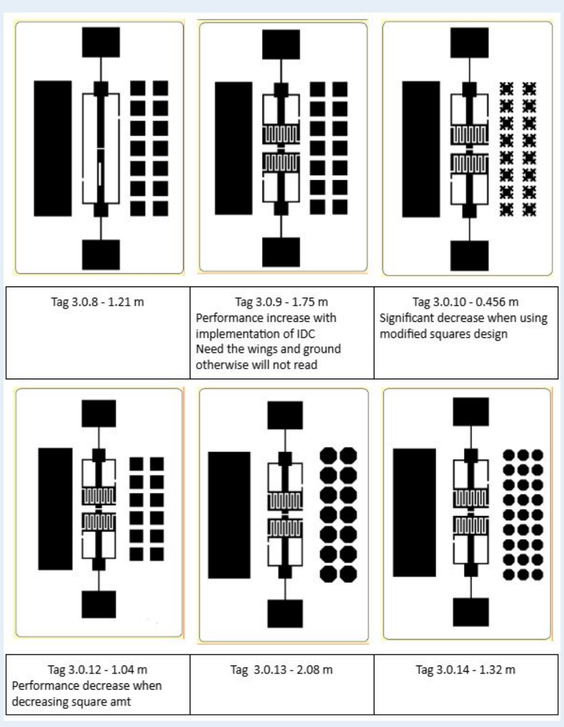


Final Tag CAD Design

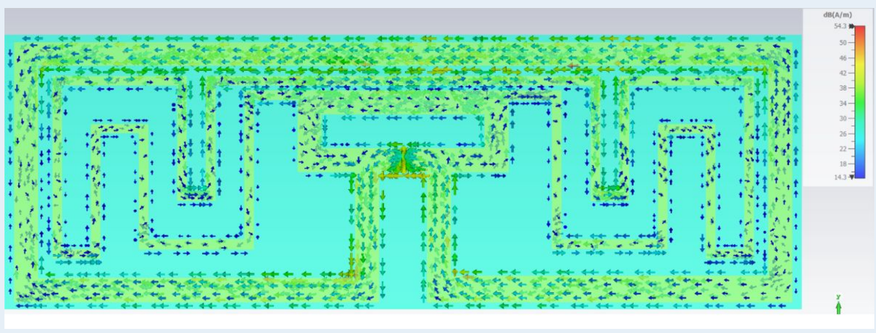


Final Assembled Tag

Testing Setup



Capacitive Gap Designs



Meandering Dipole CST Simulation

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Torque Measurement

Real-Time Stepper Motor Torque Characterization and Testing

ZEBRA

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Project Motivation

The motivation for this project comes from Zebra Technologies' need for a more compact, replicable, and efficient method of characterizing stepper motor performance. Current in-house testing systems rely on large power supplies and bulky braking mechanisms, making them difficult to duplicate across facilities. Zebra printers depend on precisely controlled stepper motors, where torque, speed, current, and resonance behavior directly impact print quality. However, limited characterization data under varying load conditions makes it difficult to predict performance issues or diagnose torque-related problems. This project addresses that gap by developing a streamlined torque measurement fixture integrating a motor under test, torque transducer, particle brake, and STM32-based control system. The fixture enables real-time measurement, visualization, and analysis of torque and speed under controlled conditions, improving motor characterization, stability, and overall system reliability.

Anticipated Best Outcome

The anticipated best outcome is a fully functional, modular torque measurement fixture capable of characterizing stepper motor performance under controlled load conditions. The system integrates STM32-based motor control, a current-regulated particle brake, and a calibrated torque transducer to generate accurate torque–speed data. A streamlined 24 V power architecture, reliable signal conditioning, and a custom 3D-printed fixture to support stable operation. A technician-friendly GUI enables real-time control, visualization, and automated data logging. The final system is designed to be reproducible, adaptable to various motor sizes, and ready for deployment across Zebra facilities.

Key Accomplishments

Torque Signal Conditioning Circuit: Designed and implemented an analog front-end to interface the ±10 V output of the torque transducer with the 0–3.3 V input range of the STM32 ADC. The circuit performs resistive scaling and introduces a mid-supply offset (~1.65 V) to center zero torque within the ADC range, enabling accurate bidirectional torque measurement. Integrated low-pass filtering (~1 kHz cutoff) reduces switching noise from the motor driver while preserving relevant torque dynamics. The circuit was simulated and validated through bench testing to confirm proper voltage mapping and stable signal acquisition (*Fig. 3*)

Particle Brake Current Driver: Developed a current-controlled driver circuit for the magnetic particle brake using an op-amp and MOSFET low-side configuration. A 0–3.3 V control signal from the STM32 DAC regulates brake current from 0–75 mA, corresponding to approximately 0.6–16 oz-in of braking torque applied to the motor. A sense resistor enables closed-loop current control, while a flyback diode protects against inductive transients. This design allows precise, repeatable load application for generating torque–speed performance curves (*Fig. 3*).

Quadrature Encoder Interface Circuit: Designed a signal conditioning circuit for the quadrature encoder outputs from the torque transducer to ensure clean and stable digital signals for the STM32. The circuit improves signal integrity and enables accurate measurement of rotational speed and direction. This supports synchronization between torque and position data and allows identification of resonance behavior and step consistency under varying load conditions (*Fig. 3*).

System Integration & Motor Control Validation: Integrated the STM32 microcontroller, DRV8424EVM stepper motor driver, signal conditioning circuit, encoder interface, and particle brake driver into a unified test platform. Electrical integration included structured wiring, shared grounding, and terminal connections to reduce noise and improve reliability. Motor control signals including step, direction, and enable were validated across multiple stepping modes, and system behavior was observed under varying load conditions. This enables coordinated motor actuation, torque measurement, and speed feedback for controlled characterization of motor performance (*Fig. 2*).

Mechanical Fixture Development: Developed and refined the mechanical test fixture, including mounting and alignment of the stepper motor, torque transducer, and magnetic particle brake. Proper shaft alignment and coupling selection minimized vibration and measurement error. The resulting fixture provides a stable and repeatable platform for torque characterization under controlled loading conditions (*Fig. 1*).

STM32 Motor Control Firmware: Developed firmware to precisely control the stepper motor using timer-generated step pulses, GPIO-based direction/enable signals, and configurable microstepping modes. Supports dynamic speed updates and ramping profiles for smooth operation and reduced missed steps. Integrated DAC control enables synchronized motor speed and particle brake loading for repeatable torque-speed testing. (*Fig. 2*)

Encoder Processing & RPM Calculation: Implemented quadrature encoder interfacing using hardware timer mode for accurate position and direction tracking with minimal CPU overhead. RPM is calculated from encoder counts over fixed intervals with filtering applied to reduce noise. Enables real-time speed feedback and stall detection, synchronized with torque measurements. (*Fig. 3*)

Data Logging: Designed high-speed USB data streaming using STM32 CDC interface to transmit torque, RPM, and test parameters in real time. Utilizes structured binary packets with timing data for accurate time-series reconstruction. Supports continuous logging for live monitoring and post-processing analysis. (*Fig. 4*)

GUI Integration & Control: Developed communication between STM32 and a host GUI for real-time system control and visualization. Users can adjust motor speed, brake load, and test parameters while receiving live torque and RPM data. Enables interactive testing and immediate performance feedback. (*Fig. 4*)

Automated Motor Characterization Tests: The system implements automated testing routines for repeatable torque-speed characterization under controlled conditions. In the baseline speed sweep test, the motor is driven across a user-defined full-step frequency range at minimal load, with step frequency incremented in fixed intervals and torque and RPM sampled at each point to generate continuous torque versus speed curves. In the progressive load test, the motor operates at a fixed speed while the particle brake load is increased via DAC control until stall is detected using encoder feedback, recording stall torque at each frequency and enabling identification of performance limits. Hardware-timed control ensures consistent dwell times and sampling intervals, while automated sequencing and encoder-based feedback provide reliable stall detection, reduced user intervention, and improved data repeatability. (*Fig. 4*)

Project Outcome

We were able to meet our anticipated best outcome by delivering a fully functional torque measurement system. The fixture provides live testing results, data collection, and a practical solution for evaluating stepper motor performance.

Figures

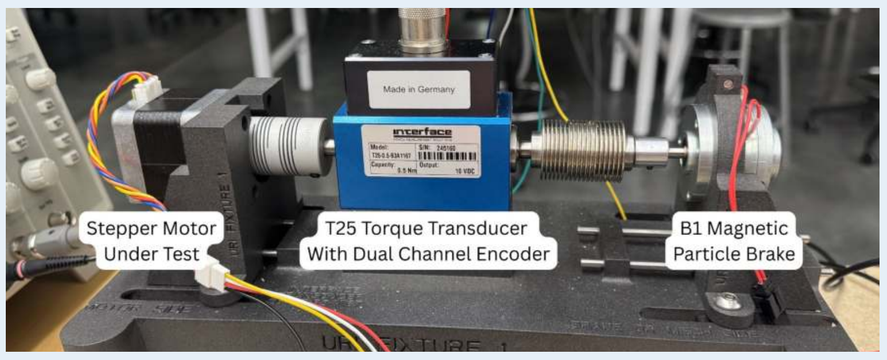

Fig. 1: Torque measurement test fixture including stepper motor, torque transducer, and magnetic particle brake

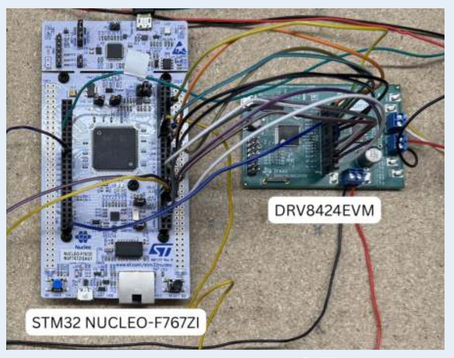

Fig. 2: Control hardware including STM32 microcontroller and DRV8424 stepper motor driver

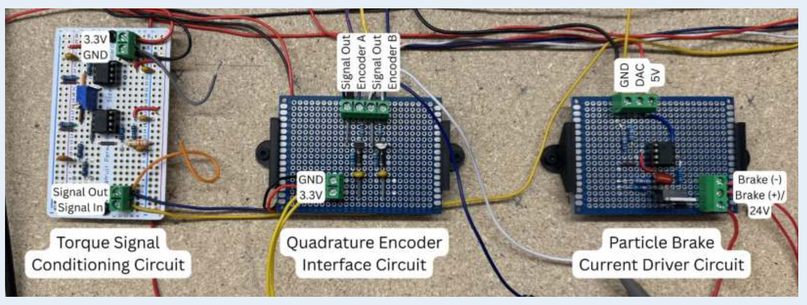

Fig. 3: Protoboard implementations including torque signal conditioning, encoder interface, and particle brake driver

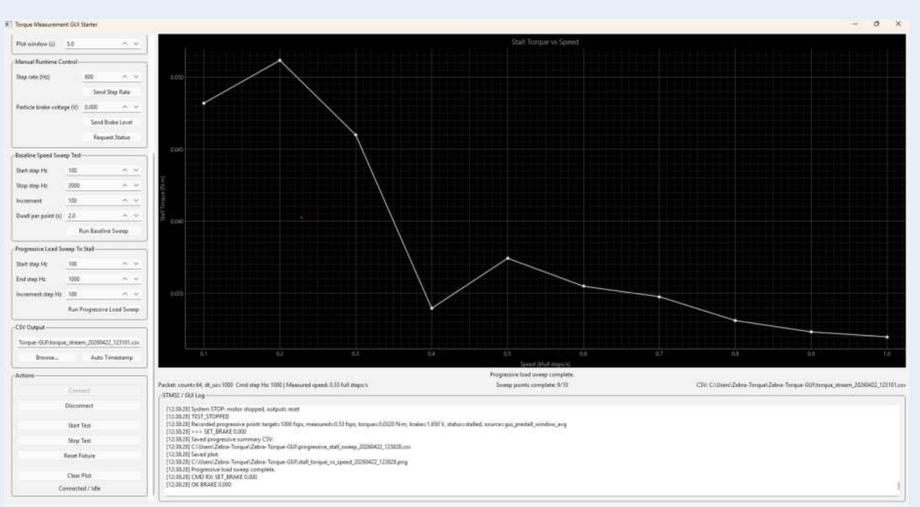

Fig. 4: Graphical User Interface for the torque measurement system

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Universal Printhead Fixture

A Universally compatible test bench fixture for thermal printhead evaluation

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Technical Directors: Morgan Malone, Dan Donato, and Joe Moreira

Project Motivation

The Universal Printhead Fixture project seeks to accelerate and improve the development cycle of Zebra Technologies thermal printhead evaluation. Currently, the qualifying process for new printheads often requires dedicated firmware and hardware setups for each model, increasing engineering time and cost. Developing a single, reconfigurable test fixture and firmware eliminates the need to design from scratch for every printhead variant, reducing the product-development cycle.
This project directly supports Zebra's goal of accelerating thermal printhead evaluation by creating a modular test environment. It integrates multiple engineering disciplines including embedded control, power electronics, and software design to simplify future testing and calibration when evaluating new printheads for Zebra products.

Key Accomplishments

- **Custom Printhead Driver PCB**: A printhead logic and power delivery board was developed to work with a wide range of printhead configurations **(Figure 1)**. With 8 lanes of data throughput and a wide thermal element voltage range, the board is capable of driving most any printhead with the correct software configurations. The I/O connections are a standard breadboard style connector type which will allow for the fast deployment of wiring harnesses to connect different styles of printhead inputs. Output logic level shifters and buffers provide a clean signal with low noise which can be changed from 3.3V to 5V with the flip of a switch.
- **Custom Motor Driver PCB:** A motor driver board was developed to interface between the XMOS board and the stepper motors needed to drive the print media through the printer fixtures **(Figure 1)**. This board uses an off the shelf drop in motor driver board, capable of being easily swapped out if a new driver should be required. The board is able to accommodate the microstepping of the stepper motors, should the fixture be needed to evaluate stepper motors alongside printheads.
- **Printhead and Motor Synchronization:** The synchronization framework between the printhead firing cycle and stepper motor motion has been developed and tested, using XMOS parallel tasks. The current process for synchronization involves choosing a speed value reliable enough for correct printing with the associated printhead.
- **Testing of Subsystems with XMOS firmware**: Diagnostic print patterns and controlled stepping sequences were performed to confirm reliable operation of all core hardware components. Timing signals, data output, and motor control behavior were verified through this testing on the latest firmware.
- **Logic and Voltage Delivery Systems Development:** Printhead voltage and logic controls vary by application (mobile, benchtop, industrial, etc.) and manufacturer. A specification was established to ensure the maximum number of printheads will work with the custom hardware and firmware solutions being developed.
- **XMOS Firmware and Real-Time Control:** A modular firmware system was developed on the XMOS platform, replacing the early Arduino-based control. Printhead, motor, and data handling are structured as parallel tasks, allowing for precise timing of data, latch, and strobe signals, while maintaining motor motion. Timing was refined through testing to ensure consistent alignment.
- **Rasterization Pipeline and Data Handling:** A rasterization pipeline was built to convert images into printhead-ready binary data. This includes basic preprocessing, bit-level formatting, and support for multi-lane data transfer. The pipeline was integrated with the firmware, allowing both code-generated tests and real images to be printed through the same system.
- **User Interface and Workflow:** A text-based UI was developed to simplify operation of the fixture. Operators can select between different printhead profiles, generate configuration files, and run the system, without modifying the firmware. This reduces setup effort while increasing efficiency.
- **Electronics Fixture:** A fixture was designed to hold the custom printhead and motor driver PCBs as well as the XMOS development board **(Figure 2)**. Front panel connectors and breadboard style heads on the PCBs allow for easy connections to printhead breakout boards which can be custom made to interface with any new printhead. Front panel I/O allows for quick selection of voltage modes and a means of turning the fixture on and off. The fixture is open, simple, and capable of future additions or alterations should new hardware be developed.
- **Printhead Breakout Connectors:** To interface between the printhead driving board and unique printhead connections, a few connector boards were designed to provide a clean and reliable connection between the standard 2.54mm pitch breadboard output from the PCB to the printhead harness. Boards were designed for the ZD6xx, ZT4xx, and ZQxx series printers, but can be easily made for additional printers in the future.

Anticipated Best Outcome

- Complete custom electronics capable of controlling any thermal printhead for use in a Zebra product (desktop, mobile, industrial), supporting configurable voltage and logic delivery.
- Firmware and PC software interfaces that allow speed control, sensor calibration, and printing with user-friendly interface.
- Successful demonstration of coordinated control between the motor, sensors, and printhead to produce a uniform printed output from a preloaded set of test prints (onboard image processing not within scope).

Project Outcome

The ABO was completed with some opportunities for further development and refinement. The Zebra provided printhead fixture will provide the opportunity to test more printheads to develop more in depth validation of the methods proposed in this project.

Figures

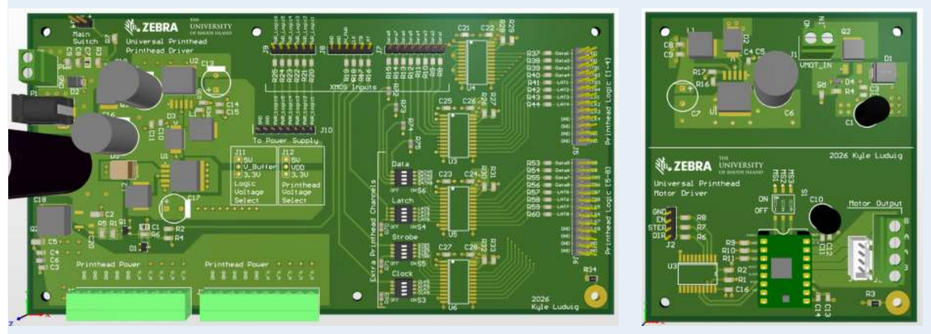

Figure 1: Custom PCB solutions for powering and connecting the XMOS development board

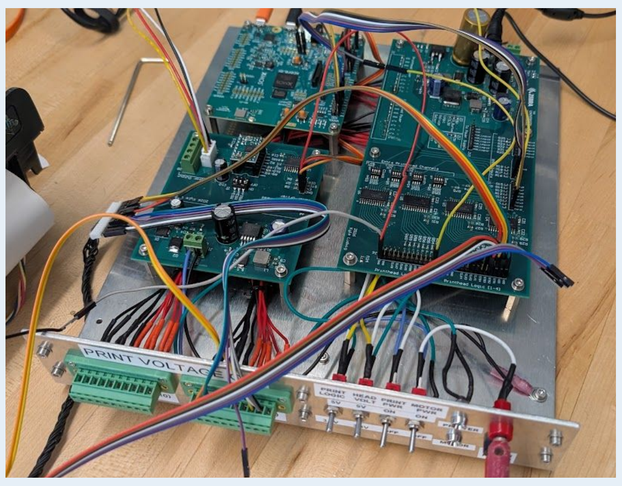

Figure 2: Complete Fixture with custom printhead operation hardware, Printhead connections, and XMOS development board.

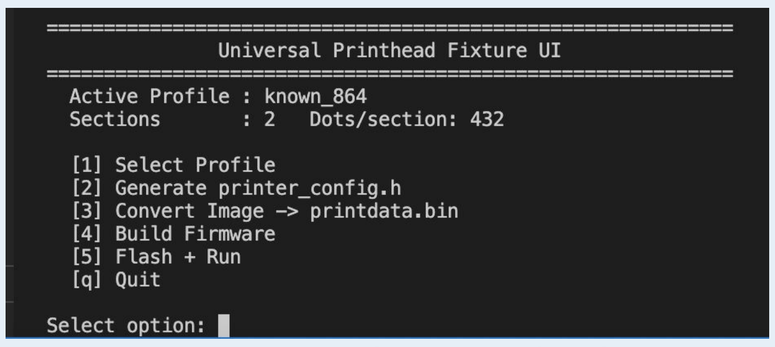

Figure 3: Python based user-friendly interface for selecting print modes, print images, and initiating the printing process.

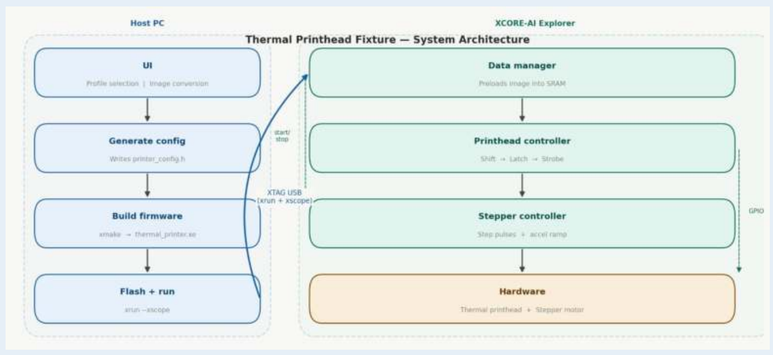

Figure 4: High-level flowchart of firmware/software architecture

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