AI-based DC Arc Fault Detection Tool

ELECOMP Capstone Design Project 2026-2027

Sponsoring Company:

University of Rhode Island Power Electronics Laboratory (URI PEL)

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Company Overview:

The University of Rhode Island Power Electronics Laboratory (URI-PEL) is conducting cutting-edge research in the field of power electronics. Our vision is to develop highly reliable and intelligent power conversion systems (PCSs) and to accelerate the design process for power electronics in various applications. Based on our strong foundation in power electronics, we have advanced various multidisciplinary research projects.

Our work has been published in distinguished journals and conference papers and is supported by various federal and state agencies, including the Office of Naval Research (ONR), the United States Geological Survey (USGS), etc., and various industries.

Technical Director(s):

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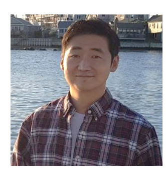

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Project Motivation:

The primary objective of this project is to develop a testbench for detecting DC series arc faults using artificial intelligence (AI)-driven detection algorithms. As the global energy sector transitions toward sustainable and high-efficiency technologies, including photovoltaic (PV) systems and electrified transportation, such as electric vehicles (EVs), aircraft, and vessels, the use of DC power systems continues to increase. However, one of the most critical safety challenges in DC power systems is the occurrence of series arc faults due to loose connections, degradation of conductors, or insulation failures, and it poses severe risks, including fire hazards, equipment damage, and potential endangerment of human life.

Unlike conventional faults, this project aims to develop an advanced DC Series Arc Fault Detection Testbench that leverages AI to enhance fault identification accuracy, enabling faster response times and improved system safety. By integrating AI-driven algorithms, this approach not only mitigates potential hazards but also contributes to the overall resilience and sustainability of modern electrical infrastructures.

Anticipated Best Outcome:

The primary outcome is a fully functional, physically realized DC series arc fault testbench. This includes a precision electromechanical arc-generation rig (linear stages/motors controlling electrode separation), a representative DC power circuit, protection circuitry (current limiting, isolation, emergency shutoff), enclosure for the protection, and an integrated sensor/DAQ chain capable of capturing high-fidelity current and voltage waveforms during both fault and non-fault conditions. Success is measured by the rig's ability to generate safe, repeatable, and controllable arc events on demand.

Beyond passive detection, the project aims to close the loop with AI-driven control: once the trained model identifies an arc signature in real time, it triggers an automated control response, such as opening a relay/contactor, de-energizing the circuit, or throttling current, within a target response window. This reframes the AI's role from a classifier alone to an embedded decision-making component within an active protection system, mirroring how a real arc-fault circuit interrupter would need to operate in the field.

Project Details:

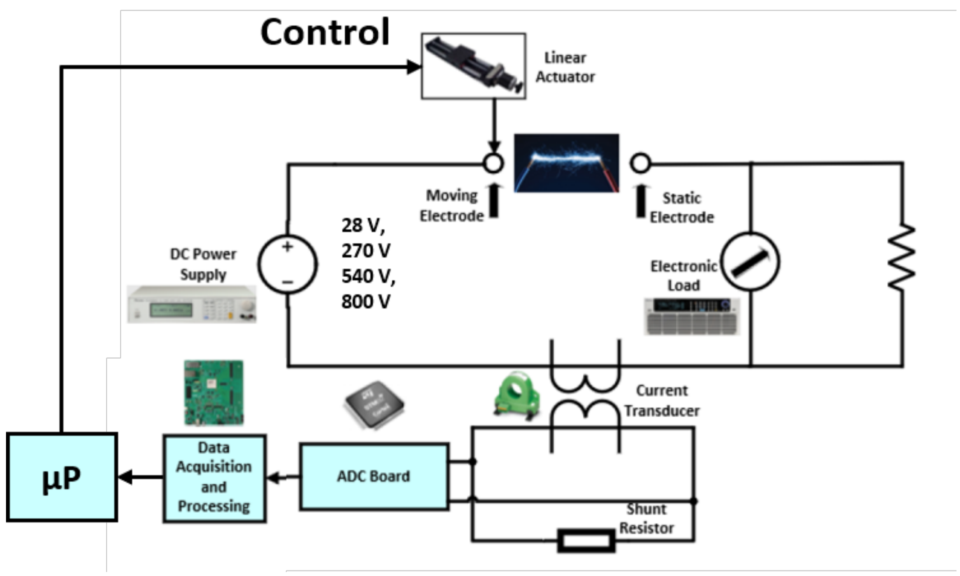

Figure 1. Overview framework of Capstone Design Project.

The testbench presented in Fig. 1 will consist of four integrated subsystems:

- Controlled Arc Generation Equipment: A linear stage/stepper or servo motor assembly that precisely separates two electrode contacts (typically carbon or copper) within a live DC circuit to generate repeatable series arc faults. Gap distance, separation speed, and contact material are controllable variables, allowing systematic generation of arcing conditions across different fault severities.

- DC Power Circuit: A representative DC source and adjustable load, wired to emulate realistic PV strings or EV battery/charging circuits, including realistic cable lengths and connector types where faults commonly originate.
- Data Acquisition System: High-sample-rate current and voltage sensors feeding into a DAQ capable of capturing the high-frequency noise signatures characteristic of arcing.
- AI/ML-based Detection: To distinguish arc events from normal transients in real time or near-real time, an AI/ML-based detection-and-control framework will be developed. This framework will process incoming current/voltage signals, extract relevant features, classify arc vs. non-arc events, and trigger an appropriate control action to safely interrupt the circuit within an acceptable response time.

Composition of Team:

Three Electrical Engineers and one Computer Engineer

Skills Required:

Electrical Engineering Skills Required:

- Power electronics and DC circuit design
- Understanding of arc fault physics
- Motor/actuator control for the mechanical arc-generation rig (stepper/servo driving, motion control)
- Sensor selection and analog signal conditioning
- PCB/breadboard prototyping for sensor interface circuits
- Familiarity with relevant safety standards (UL 1699B, NEC Article 690.11, IEC 63027)

Computer Engineering Skills Required:

- Embedded systems programming (microcontroller/FPGA firmware for real-time data capture and control)
- Machine learning/AI model development
- Software/GUI development for testbench control and live data visualization

AI Usage:

The AI Use Policy for this project is defined in Appendix A at the end of this proposal. The Technical Directors have completed the checklist in Appendix A to indicate which AI uses are permitted on this project. Any item left unchecked is not allowed.

Anticipated Best Outcome's Impact on Company's Business, and Economic Impact

This project delivers a validated, hardware-proven AI detection-and-control framework that can seed future DC arc-fault protection products. This project strengthens the lab's research portfolio by producing a validated, hardware-proven AI detection-and-control framework for DC series arc faults, a demonstrable capability that supports competitive grant proposals (e.g., NSF, DOE) and industry (e.g., RTX)-sponsored research in power electronics safety. The working testbench and preliminary dataset provide the foundation for peer-reviewed publications and conference presentations, raising the lab's visibility in the power electronics and AI/ML safety communities. It also creates a reusable experimental platform that can attract industry partnerships or sponsorships for follow-on projects and generates hands-on training data that strengthens future funding proposals by demonstrating feasibility ahead of a full-scale research effort.

Broader Implications of the Best Outcome in the Company's Industry:

A working hardware testbench with closed-loop AI detection and control contributes to a critical safety challenge in the growing adoption of PV, EV, and battery storage infrastructure, aligning the lab's work with broader efforts to make DC power systems safer and more reliable. The detection-and-control methodology developed here is transferable across related DC applications, such as EV charging, energy storage systems, DC microgrids, and data centers, giving the research broader relevance beyond a single use case. By generating experimental data on embedded AI-based arc detection and actuation, the project also contributes to the wider research community's understanding of intelligent, self-protecting power electronics, and positions the lab to contribute technical insight toward future safety standards discussions.

Appendix A: AI Use Policy – AI-based DC Arc Fault Detection Tool

Allowed

- Students may use AI tools for
  - ☒ brainstorming support
  - ☒ concept development
  - ☒ literature and publicly available documentation review
  - ☒ software development
  - ☒ debugging
  - ☒ data analysis
  - ☒ test development
  - ☒ non-proprietary paragraph editing
  - ☒ non-proprietary single-slide formatting
  - ☒ preparation of project deliverables
  - ☒ note taking or transcription of meetings
  - ☒ Others: All other project-related tasks

Not Allowed

- Using AI in violation of university policies, applicable laws, or course-specific rules identified by capstone instruction team and project-specific rules identified by the technical directors.
- Entering proprietary, confidential, personally identifiable, security-sensitive, or otherwise restricted information into an AI system without authorization.
- Submitting AI-assisted work without understanding, reviewing, verifying, and appropriately disclosing its use.
- Submitting entire documents or presentations to an AI system for editing or formatting
- Any unchecked items from the allowed list above

Requirements

- If any use is allowed, AI tools may only be used to enhance, but not replace, students’ technical reasoning, engineering judgment, and understanding. Students must be able to explain, justify, and defend all submitted designs, code, analyses, test results, documentation, and conclusions.
- During the first two weeks of the project, the student team shall work with the Technical Directors to:
    - Identify any proprietary or confidential information that may be involved in the project.
    - Determine what information may or may not be shared with AI systems;
    - Identify the AI tools, models, accounts, and configurations approved for project use; and
    - Document any project-specific restrictions or approval requirements.
- Students shall transparently document the uses of AI using the URI CYPHER AI Usage Marking guidelines (https://web.uri.edu/cypher/ai-marking/). A workshop is planned for September to familiarize students with these guidelines.
- Students retain full professional responsibility for all design decisions, analyses, implementations, testing, documentation, presentations, and final deliverables, regardless of whether AI tools contributed to the work.