Prober Error Tracking and Evaluation

Prober Error Tracking and Evaluation Resource

ELECOMP Capstone Design Project 2025-2026

Sponsoring Company:

Vicor
1 Albion Rd
Lincoln, RI 02865
http://www.vicorpower.com

Company Overview:

Vicor Corporation designs, develops, manufactures and markets modular power components and complete power systems based upon a portfolio of patented technologies. Headquartered in Andover, Massachusetts, Vicor sells its products to the power systems market, including high-performance computing, industrial equipment and automation, telecommunications and network infrastructure, vehicles and transportation, aerospace, and defense.

Technical Director(s):

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Project Motivation:

Vicor uses a variety of ATE (Automated Test Equipment) to be able to electrically test die on silicon wafers that go into Vicor's assembled parts. One type of piece of equipment used is called a prober. Probers are set up with multiple wafers and run tests on all die for each wafer. This process can take a long time and will sometimes be run overnight or over the weekend. One problem with this is that sometimes the probers will encounter an error which will halt testing until an operator comes to fix it. We want to know how often probers stop and why. From this information, we will be able to make decisions on prober repair, prober hardware improvements, prober product file settings and personnel hiring requirements.

Anticipated Best Outcome:

The anticipated best outcome (ABO) of this project is to research, design, and implement a system for collecting and displaying information about prober errors. This system will include multiple parts: data collection, data processing, database management, and data access.

Project Details:

The first stage of the system would be a routine for sending files from the prober to the network. This will require research on what files we need, how to transfer the files, and how to set up the probers to record the data required for diagnosing errors.

Fig. 1: Martek Prober similar to ones used by Vicor

The second stage of the system involves processing the files transferred from the probers into a usable format. This will involve hands on testing with the probers to find how different types of errors are processed and recorded. After establishing an understanding of what to look for, a program will need to be designed to parse data from the prober files and enter this data into a database. This will require research and understanding on database languages and management.

eventlog - Notepad

File Edit Format View Help

```
20250413.052623,*,End Wafer Processing
20250413.052623,*,REC1,WaferID=FFN457-19C3,ProdId=P042_PAD,LotID=FFN457.1_AOI,OPID=3,TPID=,TPIP=,DeviceID=
20250413.052623,*,REC2,ProbeCardID=,ProberName=PRBR10,LoadBoardName=,LotRcpID=PadProbe,WafRcpID=PadProbe
20250413.052623,*,REC3,GoodCount=2603,BadCount=253,UglyCount=0,TouchDown=1363142,SourceCass=1,SourceSlot=19
20250413.052623,*,REC011,Tester Message=
20250413.052623,*,Wafer Map Completed
20250413.052627,*,REC4,Map Name=P:\EG_ROOT\LOTS\LOT0061\WAF0018A.MAP
20250413.052627,*,Save Wafer Map To Network
20250413.052633,*,Datalog Completed
20250413.052645,*,REC660,Wafer ID=FFN457-20D0,SourceCass=1,SourceSlot=20
20250413.052645,*,Load Wafer
20250413.052646,*,REC5,DestCass=1,DestSlot=19
20250413.052646,*,Unload Wafer
20250413.052823,*,REC6,diameter=200000,refDieOffsetX=68538,refDieOffsetY=-49502,dieSizeCX=3250,dieSizeCY=3000,dieSpacingCX=0,dieSpacingCY=0
20250413.052823,*,REC7,flatOrNotch=1,FlatAngle=90,UseSecondaryFlat=0,secondFlatAngle=90,numRows=73,numCols=68,orloc=2,praxi=0
20250413.052823,*,REC8,NullBinCode=255,MCSVectorX=4,MCSVectorY=3,MCSFactorX=1,MCSFactorY=1,RefDieX=9,RefDieY=49,numBinGroup=18
20250413.052823,*,REC9,Unused_Bingroup ,12632256,2,17-30,32-1023                    ,None
20250413.052823,*,REC9,EDGE             ,0,0                                  ,UGLY   ,GOOD
20250413.052823,*,REC9,GOOD             ,3182592,1                                    ,GOOD
20250413.052823,*,REC9,Contact          ,7114940,3                                    ,BAD
20250413.052823,*,REC9,Leakage          ,3952820,4                                    ,BAD
20250413.052823,*,REC9,OCF SS           ,6316128,5                                    ,BAD
20250413.052823,*,REC9,TBG TOSC TMON    ,11837540,6                                   ,BAD
20250413.052823,*,REC9,UVLO             ,6303744,7                                    ,BAD
20250413.052823,*,REC9,OVLO             ,9449616,8                                    ,BAD
20250413.052823,*,REC9,Enable VDR OCS   ,14464008,9                                   ,BAD
20250413.052823,*,REC9,RDSON FREQ D     ,3158204,10                                   ,BAD
20250413.052823,*,REC9,SCLK RDSON TIM   ,33020,11                             ,BAD
20250413.052823,*,REC9,FLTB IMON IMON   ,13117456,12                                  ,BAD
20250413.052823,*,REC9,WRITE RETRY      ,56540,13                             ,BAD
20250413.052823,*,REC9,TON TOFF         ,3158204,14                                   ,BAD
20250413.052823,*,REC9,REGISTER DATA    ,9449616,15                                   ,BAD
20250413.052823,*,REC9,CURRENT SENSE    ,33020,16                             ,BAD
20250413.052823,*,REC9,ALARM            ,14464008,31                                  ,BAD
20250413.052823,*,REC150,Chuck Temp=35.000000,Platen Temp=29.400000
20250413.052823,*,Start Wafer Processing
20250413.112843,*,End Wafer Processing
20250413.112843,*,REC1,WaferID=FFN457-20D0,ProdId=P042_PAD,LotID=FFN457.1_AOI,OPID=3,TPID=,TPIP=,DeviceID=
20250413.112843,*,REC2,ProbeCardID=,ProberName=PRBR10,LoadBoardName=,LotRcpID=PadProbe,WafRcpID=PadProbe
20250413.112843,*,REC3,GoodCount=2411,BadCount=445,UglyCount=0,TouchDown=1365998,SourceCass=1,SourceSlot=20
20250413.112843,*,REC011,Tester Message=
20250413.112843,*,Wafer Map Completed
20250413.112846,*,REC4,Map Name=P:\EG_ROOT\LOTS\LOT0061\WAF0019A.MAP
20250413.112846,*,Save Wafer Map To Network
20250413.112853,*,Datalog Completed
20250413.112905,*,REC660,Wafer ID=FFN457-21C3,SourceCass=1,SourceSlot=21
20250413.112905,*,Load Wafer
20250413.112905,*,REC5,DestCass=1,DestSlot=20
20250413.112905,*,Unload Wafer
20250413.113044,*,REC6,diameter=200000,refDieOffsetX=68540,refDieOffsetY=-49491,dieSizeCX=3250,dieSizeCY=3000,dieSpacingCX=0,dieSpacingCY=0
20250413.113044,*,REC7,flatOrNotch=1,FlatAngle=90,UseSecondaryFlat=0,secondFlatAngle=90,numRows=73,numCols=68,orloc=2,praxi=0
20250413.113044,*,REC8,NullBinCode=255,MCSVectorX=4,MCSVectorY=3,MCSFactorX=1,MCSFactorY=1,RefDieX=9,RefDieY=49,numBinGroup=18
20250413.113044,*,REC9,Unused_Bingroup ,12632256,2,17-30,32-1023                    ,None
20250413.113044,*,REC9,EDGE             ,0,0                                  ,UGLY   ,GOOD
20250413.113044,*,REC9,GOOD             ,3182592,1                                    ,GOOD
```

Fig. 2: Example of a prober event log

The third stage of this project will be to establish a web tool to display and sort the information gathered. This web tool needs to be able to sort the data using various fields and parameters. This stage will require researching the best solution and how to integrate and display information from a database and how to query that database. This part will require some creativity from the capstone designers. The data will need to be sorted/ filtered by several different fields: date range, time range, type of error, prober number, product type. We are partnering with a prober company and they will be supporting the team with this aspect of the project.

This web tool will be integrated with an existing site run by the prober company and must follow certain design principles. These include WISP design with a RESTful style and a MVC design pattern. WISP design describes the different services used to organize the site, with WISP standing for Windows 2016 Server or Windows 10, Internet Information Server 10.0, SQL Server Database Engine, Python/PHP (with Javascript as the Paintbrush). RESTful is an architectural style for distributed hypermedia systems, and it stands for Representational State Transfer. More about REST can be found here. MVC design pattern stands for Model-View-Controller and describes the logic used when designing a website.

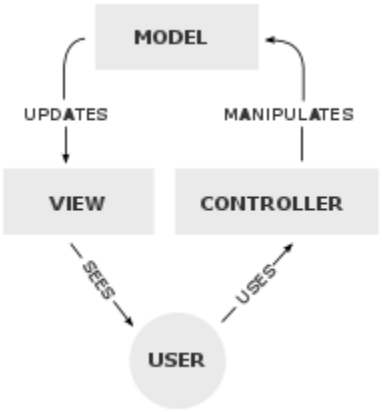

Fig. 3: Diagram of interactions within the MVC pattern

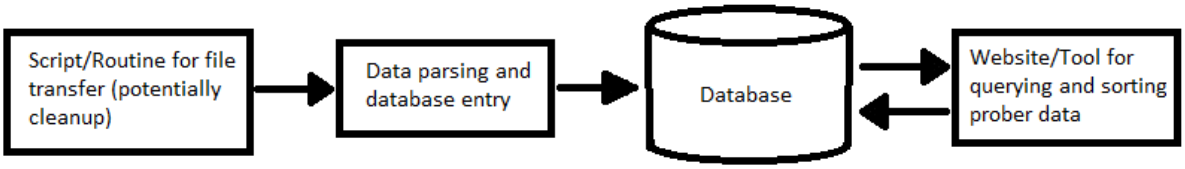

Fig. 4: Block diagram showing the structure of the proposed system

Hardware tasks include:

- Testing with prober to determine responses to different types of errors

Software tasks include:

- Creating a routine for file upload and Creating a program to parse data from files
    - Skills Needed: Python, C++, MySQL or SQLServer

- Database creation and management
    - Skills Needed: MySQL, SQLServer, or equivalent
- Website/Tool for displaying, searching, and sorting data from database
    - Skills Needed: Javascript, PHP, CSS, IIS, ASP.NET, HTTP
- Debugging and testing software

Composition of Team:

2-3 Computer Engineers **(preference will be given to those with a strong background in computer science and/or a computer science minor)**

Skills Required:

Electrical Engineering Skills Required:

- Basic Debug skills

Computer Engineering Skills Required:

- Python scripting and file handling (Python, C++)
- Database setup and querying (MS-SQL, MySQL)
- Website design, API Development (HTML, CSS, JS, PHP, RESTful, ASP.NET, IIS)
- Basic Network understanding

Anticipated Best Outcome's Impact on Company's Business, and Economic Impact

Should the ABO be achieved, it will allow us more efficiently test our parts and better understand and prepare for prober errors.

The end use of this project could enable:

- Prober utilization/ efficiency
- Provide guidance on prober repair and maintenance
- Identify off-shift personnel hiring needs
- Identify product issues
- Capacity matrix

Broader Implications of the Best Outcome on the Company's Industry:

Having a tool to track and evaluate the status of probers would be valuable to the semiconductor companies that use probers. This tool could be rolled into the toolbox provided by the probe manufacturers and would allow operations to monitor their test floor more effectively and make decisions on capacity.