Power MOSFET Modeling & Evaluation

Power MOSFET Multi-tool Modeling & Evaluation using AI

ELECOMP Capstone Design Project 2026-2027

Sponsoring Company:

Vicor
1 Albion Rd
Lincoln, RI 02865
http://www.vicorpower.com

Company Overview:

Vicor Corporation designs, develops, manufactures and markets modular power components and complete power systems based upon a portfolio of patented technologies. Headquartered in Andover, Massachusetts, Vicor sells its products to the power systems market, including high-performance computing, industrial equipment and automation, telecommunications and network infrastructure, vehicles and transportation, aerospace, and defense.

Technical Director(s):

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Project Motivation:

Vicor has developed a proprietary family of Power MOSFET or "DFET" products. Each DFET is designed for a specific switching speed, input voltage and RDSon conduction. These DFETs are now being used in many different module products. The module designers need to simulate performance of their designs and require accurate performance of the DFET simulation models. The performance metrics for the models must include variations with voltage (gate, drain, source, bulk), temperature, process, lifetime degradation and mechanical stress. In addition, these models must be adapted to a variety of simulation tools, namely, Cadence Spectre, HSPICE, QSpice (formerly LTSpice) and SiMetrix.

Anticipated Best Outcome:

The best possible outcome of this project would include this list of major accomplishments:

1) A systematic, efficient and well documented method of characterizing Power MOSFET (DFETs) that is available to both Vicor and the URI IC Lab.
2) Full evaluation of the three designs provided to the Capstone students.
3) A systematic, efficient and well documented method of creating models for Cadence Spectre, HSPICE, QSpice and SiMetrix – with a possible "bridge" software that can convert on model to the other.
4) Demonstration that each model matches the evaluation data over voltage, temperature, time and stress.

Project Details:

Project chiefly involves measuring, evaluating and modeling three Power MOSFET types from Vicor Corporation. Below is an example of datasheet cover page for one of the Power MOSFETs:

N-Channel 70V Power MOSFET

PIF13N70

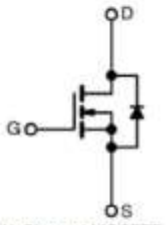
The PIF13N70F is a single 70V, 19mΩ, chip-scale, N-channel Power MOSFET. The device uses technology that uniquely integrates Vicor custom DFET technology and WLCSP fabrication processes. The chip scale package offers small area, frontside Drain, low vertical profile and is fully compatible with standard SMT assembly processes.
The PIF13N70F device offers low on - resistance and total gate charge, outperforming conventional trench MOSFETs and enabling high frequency, low voltage switching. The device offers high power density, reducing the board sizeof DC/DC converters and other power management systems.
The Chipscale construction reduces parasitic inductance found in traditional trench FETs where the Drain is on the opposite side of the die from the Source.

Features

- Industry leading figures of merit: $r_{DS(ON)} \times Q_g$ and $r_{DS(ON)} \times Q_{gd}$
- Low profile/small footprint chip scale WLCSP package
- Low output capacitance as well as low gate charge
- Low Inductance
- Low Gate Resistance
- High frequency switching
- Low thermal resistance

Applications

- Synchronous rectification
- High power density DC/DC
- Primary side switch
- Bus converters

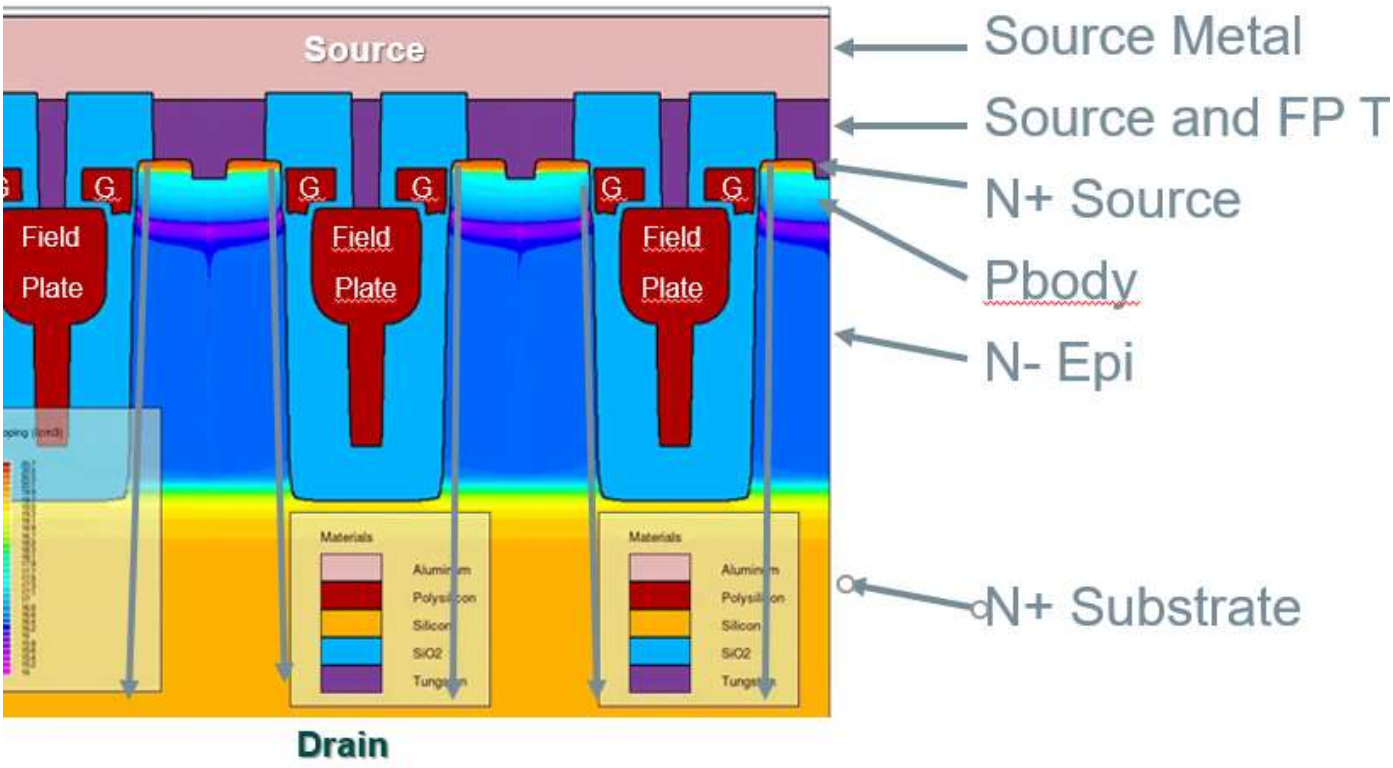


N-Channel MOSFET

$I_{D\ continuous}$	T_A = +25°C	13A	Maximum
$I_{D\ Pmax}$	T_A = +25°C	35A	Maximum
$V_{(BR)DSS}$	I_D = 1mA	70V	Minimum
$r_{DS(ON)}$	V_{GS} = 5V	19mΩ	Typical
Q_g	V_{GS} = 5V, I_D = 4A	4.5nC	Typical
Q_{gd}		1.2nC	Typical

Project Details (continued):

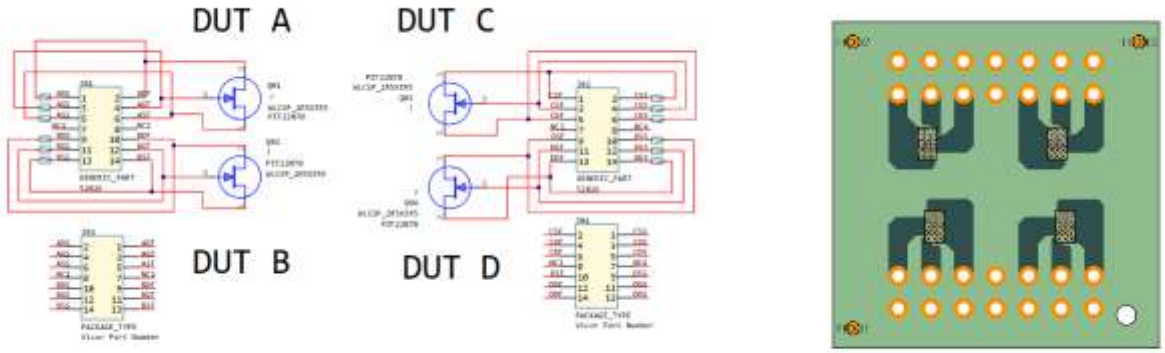
A side view of an industry standard version of a Power MOSFET called a “TrenchFET” is shown below:



The paper “The Trench Power MOSFET: Part I – History, Technology, and Prospects” by Williams, et. al. in “IEEE Transactions on Electron Devices, VOL. 64, No. 3, March 2017” is very helpful.

Project Details (continued):

In order to create measurements for the product, the Capstone team will be provided coupon boards with 4 die per board and a schematic for creating connections to test equipment:



Vicor will provide at least 20 coupon boards for each of the 3 DFET variants.
Once the materials are provided, Dr. Kim and the Vicor Technical team will provide guidance on the type of electrical curves needed to create DC, AC, Transient and Temperature model parameters. A bulk of the first half of the Capstone program will be investigating the correlation between model parameters required for different simulators and the lab curves required to attain those parameters. A very good primer would be to have the book "Semiconductor Device Modeling with SPICE" by Giuseppe Massobrio and Paolo Antognetti.

The first half of the year should also be spent learning about the simulation software and setting up "off the shelf" models for Power MOSFETS with that software.

Lastly, the first half of the year should be spent learning how to program the respective lab equipment required to measure the Vicor devices. Also, software preparation should be completed for data analysis.

Work in the second half of the year will be to combine all the measurement and software skills with model and evaluation skills. The team will develop an iterative process, with the help of Dr. Kim's AI toolset, to efficiently match simulation and model performance with extracted evaluation data. Ideally, simulation vs. data is matched for all listed EDA tools.

Project Details (continued):

Composition of Team:

At least 2 Electrical Engineering students with emphasis in semiconductor physics and materials and 1 Computer Engineering student with emphasis on scripting for lab equipment and file conversion

[Hardware/Electrical Tasks:]

- Learn Semiconductor Analysis tool in URI IC Lab
- Take basic IV Curve MOSFET measurements by using analysis tool
- Create test benches in Simulation tools (Cadence Spectre, SiMetrix, QSpice/LTSpice)
- Refine test benches with advisors (voltage, ac, transient, stress, lifetime)
- Develop 'simplified' models for Power MOSFETS and run test benches
- Translate simulation test benches to actual Lab evaluation benches
- Take evaluation data on all Vicor products
- Process data for model creation
- Run new simulations, compare with data, rinse and repeat.

[Firmware/Software/Computer Tasks:]

- Ensure that computers can communicate properly with all required lab equipment
- Assist with tool installation and training (Cadence Spectre, SiMetrix, QSpice/LTSpice)
- Study model formatting and translation – is it possible to design a model in one format and have the other formats "automatically" generate?
- Create automation for translating lab evaluation curves to model parameters
- Work with Dr. Kim on AI model/data iteration algorithms
- Create easy to use environments for data collection and analysis, tool use and incorporation into presentations

Skills Required:

Electrical Engineering Skills Required:

- Understanding of power semiconductors
- Good lab and equipment skills – especially in kelvin sensing, significant digits and repeatability
- Understanding of semiconductor physics and translation into typical MOSFET/DFET models

Computer Engineering Skills Required:

- Good understanding of scripting required for lab equipment
- Familiarity with Python programming
- Familiarity with AI use in optimization algorithms
- Good understanding of file translation, format conversion and encryption (model encryption is a nice to have feature for IP protection)

AI Usage:

The AI Use Policy for this project is defined in Appendix A at the end of this proposal. Technical Directors: complete the checklist in Appendix A to indicate which AI uses are permitted on this project. Any item left unchecked is not allowed.

Anticipated Best Outcome's Impact on Company's Business, and Economic Impact

Vicor can design and release more and varied module product as the DFET portfolio grows. The faster we can evaluate and model these new DFET devices, the faster Vicor can grow market share and generate revenue. Furthermore, the ability predict DFET behavior over all conditions enables better prediction of specification margins – eliminating "fat" from key specifications, creating more reliable products and generating more high value/profit business.

Broader Implications of the Best Outcome on the Company's Industry:

Vicor is a market leader in high performance power supplies. The faster Vicor can develop smaller high efficiency product, the faster our customers can adopt that technology and improve end product. As the industry grows, other companies will also have to improve their performance. In order for the industry to improve performance they will have to have 'quick turn' evaluation and prediction of power devices.

Appendix A: AI Use Policy – DFET Multi-tool Modeling & Evaluation using AI

Allowed

- Students may use AI tools for

  ☐ brainstorming support

  ☐ concept development

  ☐ literature and publicly available documentation review

  ☒ software development

  ☒ debugging

  ☒ data analysis

  ☐ test development

  ☐ non-proprietary paragraph editing

  ☐ non-proprietary single-slide formatting

  ☒ preparation of project deliverables

  ☐ note taking or transcription of meetings

  ☐ Others: _____

Not Allowed

- Using AI in violation of university policies, applicable laws, or course-specific rules identified by capstone instruction team and project-specific rules identified by the technical directors.
- Entering proprietary, confidential, personally identifiable, security-sensitive, or otherwise restricted information into an AI system without authorization.
- Submitting AI-assisted work without understanding, reviewing, verifying, and appropriately disclosing its use.
- Submitting entire documents or presentations to an AI system for editing or formatting.
- Any unchecked items from the allowed list above.

Requirements

- If any use is allowed, AI tools may only be used to enhance, but not replace, students' technical reasoning, engineering judgment, and understanding. Students must be able to explain, justify, and defend all submitted designs, code, analyses, test results, documentation, and conclusions.
- During the first two weeks of the project, the student team shall work with the Technical Directors to: identify any proprietary or confidential information that may be involved in the project; determine what information may or may not be shared with AI systems; identify the AI tools, models, accounts, and configurations approved for project use; and document any project-specific restrictions or approval requirements.
- Students shall transparently document the uses of AI using the URI CYPHER AI Usage Marking guidelines (https://web.uri.edu/cypher/ai-marking/). A workshop is planned for September to familiarize students with these guidelines.
- Students retain full professional responsibility for all design decisions, analyses, implementations, testing, documentation, presentations, and final deliverables, regardless of whether AI tools contributed to the work.