Scan Head System Controller

Polygon Scan Head Integration with System Controller

ELECOMP Capstone Design Project 2019-2020

Sponsoring Company:

Cambridge Technology
125 Middlesex Turnpike, Bedford, MA 01730
http://www.cambridgetechnology.com/

Cambridge Technology is continuing support of the Program for the 2nd consecutive year:
https://web.uri.edu/elecomp-capstone/project-details-by-team-2018-2019/cambridge-technology/

(The team won 2nd Prize at the Summit held on May 10th, 2019)

Company Overview:

Cambridge Technology designs, develops, and manufactures leading-edge laser beam steering solutions including galvanometer and polygon optical scanning components, 2-axis and 3-axis scan heads, scanning subsystems, high power scanning heads, and controlling hardware and software. Our company partners with OEM customers to deliver scanning solutions that support advanced industrial processes, electronics, and laser-based medical applications.

As the inventor of galvanometer-based optical scanning technology, we make it our mission to drive innovations in photonics by delivering unprecedented technical capabilities through the critical lens of collaboration, quality, and customer service. We dedicate ourselves to excel at:

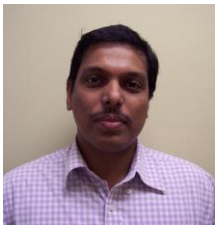
Collaboration with our partners to ensure our goals and pathways align

- Innovation to bring tomorrow's beam steering solutions to life today
- Engineering to perfect our products and our processes
- Delivery from the largest engineering solution to the smallest component

Technical Directors:

Mark Lucas
Manager, Software Engineering
Mark.Lucas@cambridgetechnology.com

Seetharam Sivam
Senior Embedded Firmware Engineer
Seetharam.Sivam@cambridgetechnology.com



Gary Buker
Senior Electrical Engineer
Gary.Buker@cambridgetechnology.com

Project Motivation:

Cambridge Technology offers Galvo based laser scanner solutions, which typically consist of a two-axis scan head, servos drivers, a laser steering controller and end user software application. All of our controllers are designed to easily integrate with either an Application Programming Interface (API) or ScanMaster Designer (SMD) software from Cambridge Technology. The ScanMaster Controller (SMC) offers a wide range of programmable control signals that provide flexibility in laser control that is synchronized with galvanometer motion and positions.

Our plug-and-play interface allows for easy connection to commonly used lasers. Our ScanMaster Designer (SMD) software is simple to use and features a graphic design environment with an intuitive user interface. The software uses standard file formats and features a wide range of editing tools for easy job creation. ScanMaster API provides access to most of the SMD functionality through end customers own user interface. All of our controller and software products can drive any of our galvanometer XY scanner sets and scan heads.

Even though bit-map raster imaging is supported by SMD and SMC using galvanometer-based scan heads, we are looking to extend the capabilities of these two subsystems to drive our new polygon-based scan head. Polygon based scan heads have the potential of performing bit-map imaging at much higher speeds and much higher pixel resolution.

Figure 1: Scan Master Controller. Galvo Scanner and Laser controller.

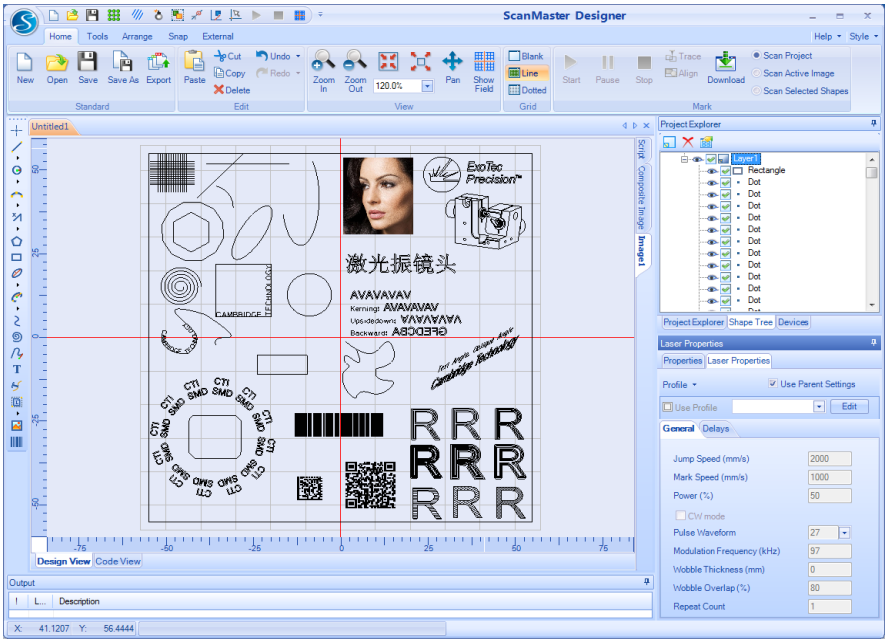


Figure 2: Scan Master Designer software used for a variety of laser processing applications.

Anticipated Best Outcome:

1. Development of FPGA custom logic and associated embedded firmware that processes and delivers precise bit-map raster data streams to the laser synchronously with the polygon rotation in order to properly reproduce a bit-map on a target substrate.
2. The creation of a data entry GUI interface extension to SMD for polygon scan heads to permit the input the new parameters associated with polygon scanning.
3. Integration of the control algorithm into the SMC processing system and the development of demonstration jobs using SMD for the polygon scanner system.
4. Creation of an algorithm that takes calibration correction data and creates a position profile that moves the distortion correction galvanometers into the proper correction locations in real time.

Project Details:

The project will be developed and tested using the existing Cambridge Technology SMC hardware platform. Firmware source code will be provided as a basis for the development effort. A polygon scanner system with a diode laser will be used to debug the logic and interface electronics. Final integration and demonstration of results will be performed at CT facilities where an actual marking laser will be used.

Overall System Concept:

The SMC/SMD have been designed to control galvanometer scan heads primarily in a vector mode. They do have the ability to control galvanometer scan heads in a raster mode but this does not currently work with polygonal scan heads. Polygon scan heads only operate in a raster mode so vector scanning is not an option. In a polygon scan head the polygon cannot change speed quickly so it is the master clock. The laser will either be a slave to the polygon head and output pulses when commanded or phase sync to the Start of scan signal from the head. Another mode can be used where the laser internal seed clock is used to phase sync the polygon scan head to the laser using the X- galvanometer.

The polygon scan head can be configured three ways. It can have no galvos and operate as a line scanner similar to a laser printer. It can have one galvanometer to provide the slow scan axis or it can have two galvanometers and correct for lens distortion and phase syncing.

Figure 3 shows a block diagram of the signals that are used to control the polygon scan head.

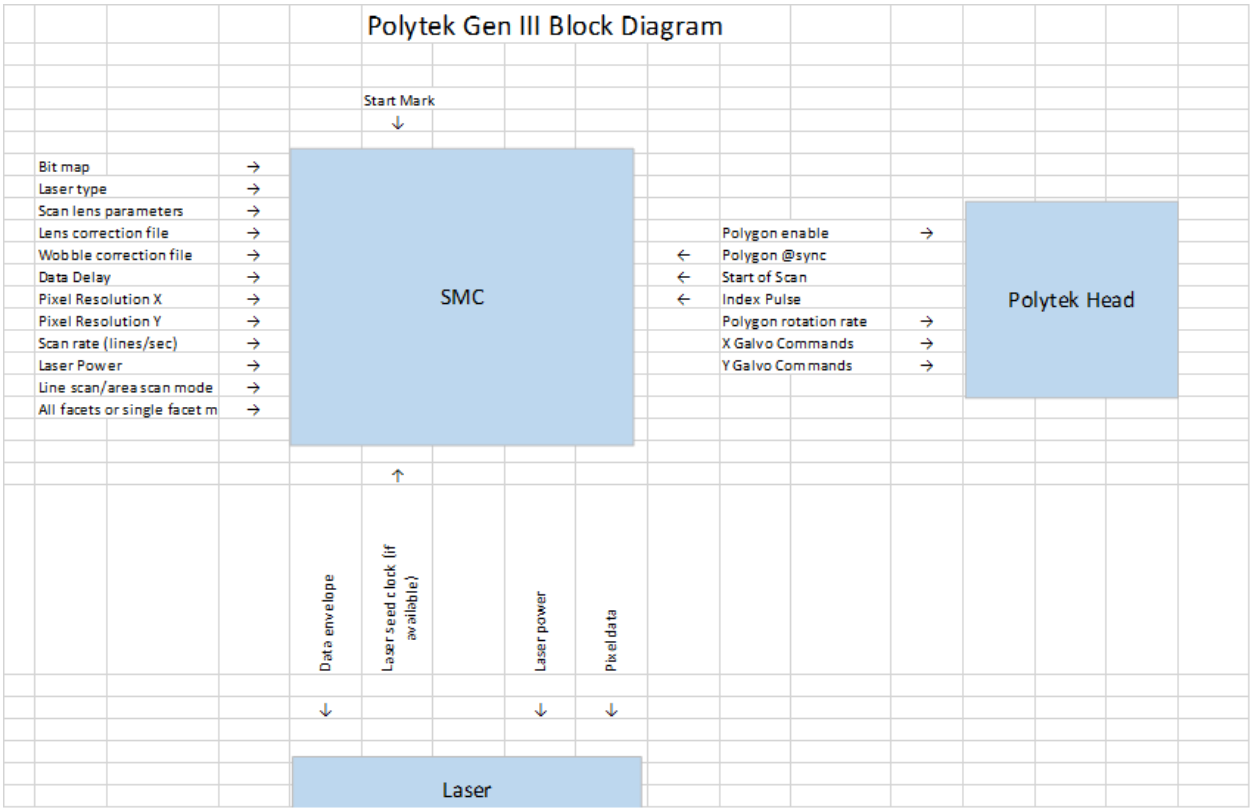


Figure 3: System Block diagram for Cambridge Technology polygon scanning system.

In the final product configuration utilizing the result of the project work, the polygon scan head would interface directly to dedicated ports on the SMC hardware platform.

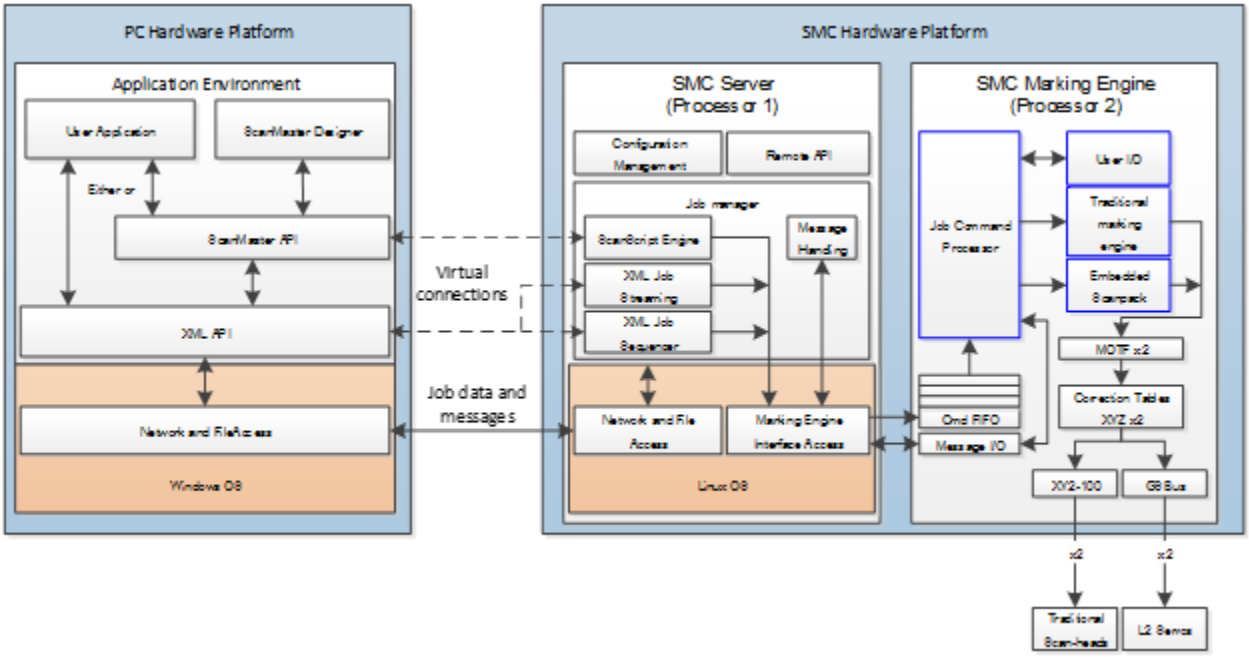


Figure 4: SMC & SMD Architecture overview.

The diagram in Figure 4 shows the distributed multi-processing arrangement of the SMC and associated Windows host base software and APIs. The project work involves development of configuration software that runs on the PC as part of ScanMaster Designer. This is code written in Microsoft C#/.NET. Bit-map processing code written in C/C++ will be deployed on the Processor 1 element of the SMC that runs a Linux OS with CT custom application software that implements the high-level control and sequencing operations. Finally, C code and Verilog FPGA code will be written that runs on the Processor 2 element of the SMC. This code handles the real-time mapping of the bit-map data to laser firing commands.

A preliminary timing diagram showing some of the signals is shown in Figure 5.

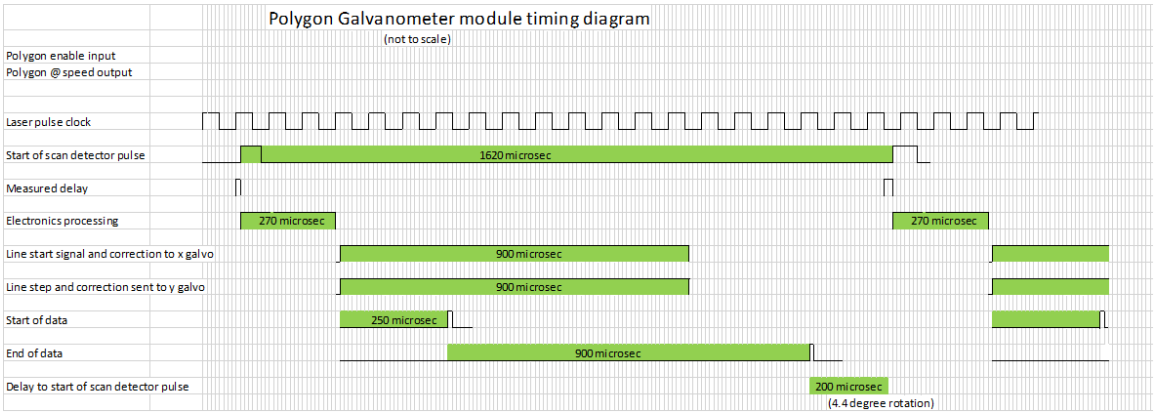


Figure 5: Preliminary timing diagram

Hardware/Electrical Tasks:

1. Procure materials and equipment
    a. SMC controller and power supplies (from CT)
    b. Basic two-axis scan head with laser pointer to illustrate basic SMD/SMC raster capability (from CT)
    c. Polygon scanner (from CT)
    d. Multi-channel oscilloscope/logic analyzer (from URI?)
2. Design and build cabling and other necessary signal conditioning circuitry to interface the polygon scan head to the SMC.
3. Research existing raster processing algorithms implemented in SMD and SMC to become familiar with the core technology.
4. Working with the SW partner, design new data structures and processing logic to support binary (single bit per pixel) output
5. Define, design and simulate the binary bit map handling logic in Verilog.
6. Support the SW effort to integrate and test the overall functionality of the system.

Firmware/Software/Computer Tasks:

1. Research existing raster processing algorithms implemented in SMD and SMC to become familiar with the core technology.
2. Research how configuration data is managed in SMD and SMC in preparation for developing a new configuration data capture GUI for polygon scanner specific data.
3. Set up and configure the SMC software development environment for the Zynq-based embedded processor including an appropriate source control system (suggest SVN and Tortoise client).
4. Develop the polygon scanner configuration editor GUI.
5. Update the raster laser property editor pages to capture polygon scanner specific process data.
6. Update the raster processing drivers in the SMC firmware to handle binary bit-map data.
7. Develop SMD demo jobs to illustrate raster processing capability.
8. Support the HW effort to integrate and test the overall functionality of the system.

Composition of Team:

- 1 Electrical/Firmware Engineer
- 1 Computer/Software Engineer

Skills Required:

Electrical Engineering Skills Required:

- FPGA fabric design and simulation using Verilog
- C code development in support of FPGA fabric manipulation in a non-OS environment
- I/O interfacing including optical isolation and digital signal termination
- Cabling and interconnect design of high-speed digital signals
- System Design & Integration

Computer Engineering Skills Required:

- Bit-map raster handling and processing in a C#/.NET environment
- C# and Microsoft WPF user interface design techniques in a Windows environment
- C/C++ application development in a Linux environment

Anticipated Best Outcome's Impact on Company's Business, and Economic Impact:

Adding this control capability to our SMC product allows our company to control the development direction of our polygon based scan heads. Currently the control system is provided by a third party. Using the SMC/SMD control solution will increase sales by enabling our customers to move into polygon scan solutions using a common interface they are familiar with.

Broader Implications of the Best Outcome on the Company's Industry:

A rough estimate for the economic benefit enabled by this feature is $500k- $800k generated through additional system sales into emerging markets that require this technology.