Gen-2 SPEC Tester
(System Power Extended Cycling)

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PROJECT MOTIVATION:

DC-DC converters must provide steady power to large processing units and as power demands are increasing, competition to make the most effective and efficient devices pushes innovation forward. Once many of the logistics of a design have been determined, minor modifications can be made in order to further optimize the performance of the design. These could be changes in the layout of MOSFETs on the chip, supporting hardware, or changes in semiconductor structure or doping levels. Testing racks are used to test sets of these chips, each divided into groups. These IC's are placed under heavy demands and held under identical conditions in order to maintain a controlled testing environment. The results of these tests can further the development of these chips. This project is motivated by the need for an efficient, compact, testing rack that can both control the conditions between chips and accurately report data. This will allow Infineon engineers to properly interpret the results and to work towards the best outcome for their DC-DC converters.

ANTICIPATED BEST OUTCOME:

By April 13th, 2018 we anticipate to have implemented a complete system capable of monitoring and managing the entire SPEC (System Power Extended Cycling) testing platform. The features/functions of this system will include the following: Telemetry data consolidation and management for 60+ I2C devices, thermal management and monitoring of local cooling fans, load control, support for different cycling modes for input power and channel enabling/disabling, and fault management through use of text/email alerts along with channel isolation and E-Fuse control. All of these features/functions will be controlled using a graphical user interface specifically designed and programmed for this system.

IMPLICATIONS FOR COMPANY AND INDUSTRY:

The successful completion of this project has the potential to give Infineon a significant advantage in the switch-mode power electronics industry. Using the SPEC testing platform, Infineon engineers will be able to precisely test multiple design configurations of their DC-DC converters both quickly and effectively. By monitoring the individual performance of each device, the team at Infineon will be able to determine the optimal characteristics for their devices performance and efficiency. With this system, Infineon will be able to actively stay ahead of their competition in the power electronics industry.

PROJECT OUTCOME:

The Anticipated Best Outcome was not achieved. VHDL designs created to communicate with SPEC platform using FPGA; also developed PC-based GUI to display telemetry data; developed backend software for communication between GUI and FPGA.

KEY ACCOMPLISHMENTS:

Waveform Generator Board: The circuit schematic for the DAC board was implemented on a standalone waveform generation card. This separate Printed Circuit Board is sized to plug directly on top of the Cyclone V DE10-Nano into its GPIO headers. While the design was initially intended to be implemented as a revision to the main system board, Infineon engineers felt a dedicated card would allow for more customization in the system. Rather than using the ATX power net of the mainboard, this card now runs of the 5V supply provided by the FPGA as it has low power requirements. Waveform generation will be customized via the SPI controller on the FPGA. Waveforms will generally be trapezoidal, with customizable rise/fall times and duty cycle for the duration of extended stress testing. However, this board is extremely modular, and any wave pattern can be programmed into its local SRAM.

I2C Controller: In order to communicate with the SPEC testing platform a VHDL design built to run on the FPGA was created. The primary purpose of the I2C controller was to communicate with the load board controller and obtain telemetry data on a regular interval from multiple built-in registers. The primary architecture of the controller was based around a finite-state machine so that users can easily debug the controller by examining individual states to observe each phase of communication. After finalizing the initial design, multiple additional versions were created to communicate with several registers simultaneously as well as take commands directly from our PC GUI.

SPI Controller: Sending commands to the waveform generator board required communication over an SPI bus therefore an SPI controller design was also created in VHDL to run in parallel with the I2C controller. The SPI controller followed the same methodology of the I2C controller by using a finite-state machine as the primary backbone of its underlying architecture. While the I2C controller communicates directly with onboard registers to obtain telemetry data, the SPI controller communicates directly with the DAC on the waveform generator board in order to define the specifics about the current transients to send to the load board. Establishing this communication with the waveform generator board over SPI using the FPGA will allow users to easily send customizable current transients to the load board using our PC GUI.

GUI Development: The GUI provides the end user with a simple way to control the testing boards and to view the data collected from each of the boards in real-time. Clicking on one of the boards displays its data, including, but not limited to, its voltage, current, power consumption and temperature. The GUI also offers the user a selection of tests to run on the boards. The user can choose to run tests on individual boards, on ten board testing neighborhoods, or on the entire rack of sixty boards.

System Overview/Flowchart of final deliverable product

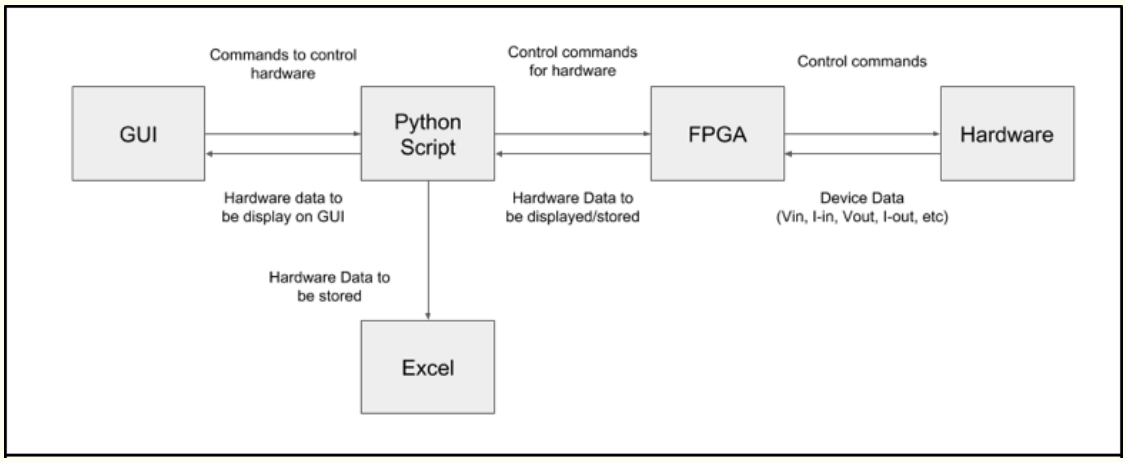

Fig 1: System flowchart of final deliverable product

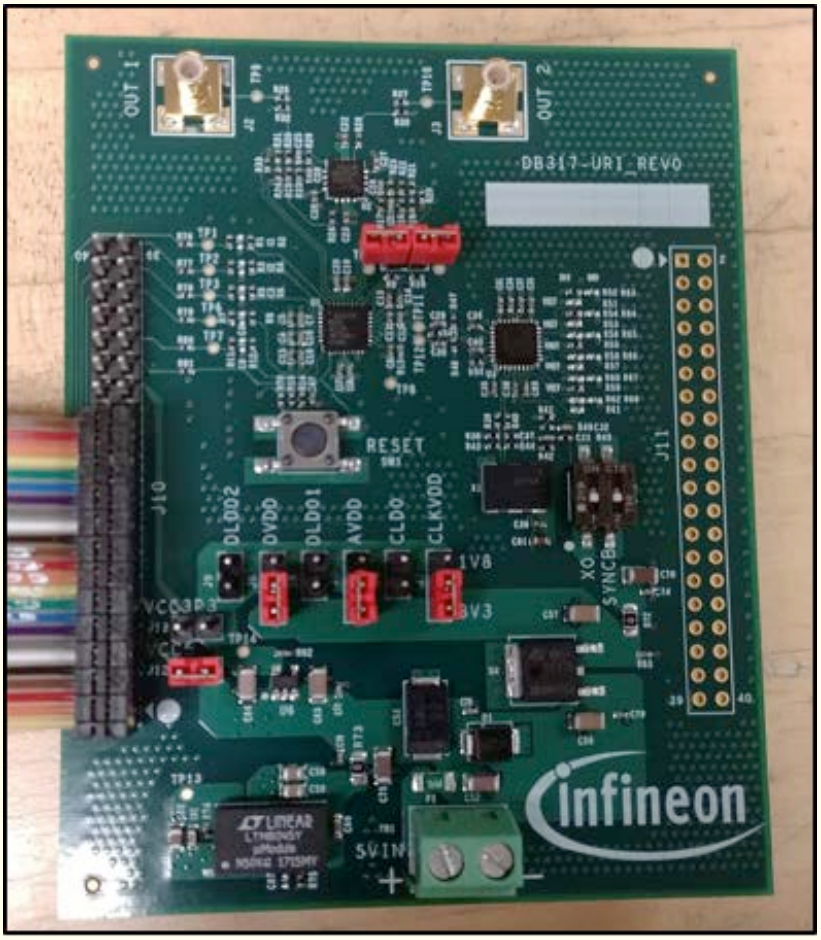

Fig 2: Waveform Generator Board

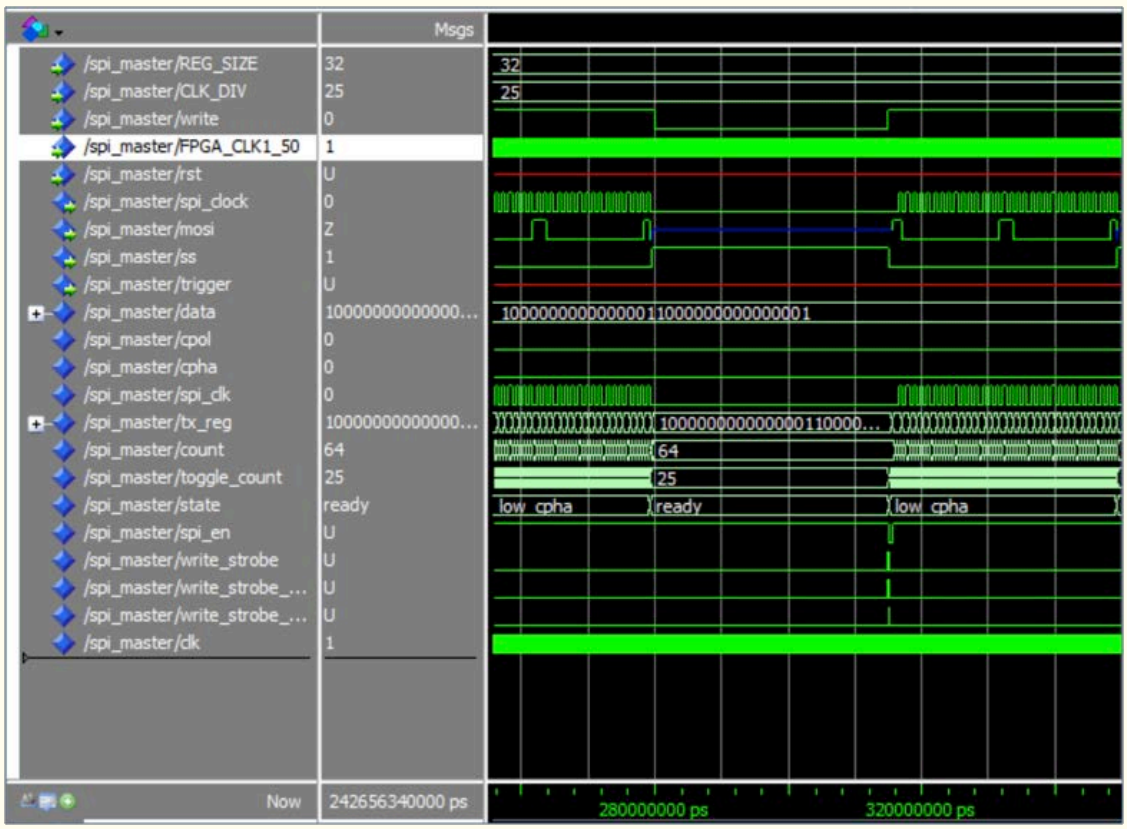

Fig 3: ModelSim Simulation of SPI Controller

Fig 4: GUI to control and monitor 60 devices