Fiber Optics Design High Voltage Equipment Control System Interface

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TECHNICAL DIRECTORS:

Sandro Silva
Mike Guerra
Mike Smith

TEAM MEMBERS: (L to R)

Mike Smith
Sandro Silva
Zackery Duclos (E)
Chris Francis (E)
Harish Sunak
Stephen Simo

PROJECT MOTIVATION:

Electromagnetic interference threatens signal transmission and reception in copper wires. The current power grid is rarely shielded from electromagnetic interference (EMI), which makes it particularly vulnerable to terrorist attacks and other serious equipment failures that could leave entire cities or counties without power for weeks. In modern times, people are extremely dependent on electricity; no power for a week could prove fatal. Fiber optic cables are immune to EMI and provide a reliable and effective solution. Fiber provides pronounced signal quality while also not conducting electricity. Fiber is also resistant to fluctuations in temperature and can be directly placed in water without affecting the signal that it's carrying. The glass core makes tampering with fiber optic cables impossible therefore offering a higher level of security. Fiber optics are a safer, more rugged alternative to copper cabling especially in electrical facilities. Utilizing fiber optics is the next step to revolutionizing and modernizing the power transmission and distribution industry.

ANTICIPATED BEST OUTCOME:

The best outcome of this project by the end of the spring semester will be to have a functional prototype interface control system. The control system will operate with two distinct control cards. First, the master control card will interface with the previous control power hub to drive indications and relay state changes to its counterpart. The other distinct card will detect changes in connectivity, adjust relays states, and report back to the master card via the fiber. This design will have additional connections for future signals and enough extra memory for any future programming.

IMPLICATIONS FOR COMPANY AND INDUSTRY:

The prototype will begin the push for American power companies to add additional security measures to protect power transmission and distribution facilities from EMI and terrorist threats. Phoenix Electric Corporation (PEC) will add to their marketability by adding this unique product not offered in most American markets. The product may also encourage PEC suppliers to make products to assist PEC in this new market once the control system is deployed. The Fiber Optic interface system will give PEC an exclusive edge against their competitors while providing heightened security and safer installation at a reasonable cost.

PROJECT OUTCOME:

The Anticipated Best Outcome was not achieved. The PCBs still need to be fabricated and VHDL tested.

KEY ACCOMPLISHMENTS:

Simulate Major Circuits: Vital circuits in our design have been simulated to ensure proper functionality. An electric rule check has been performed to make sure there are no open or short circuits within the design.

Generate Schematic for High Voltage Equipment Board: The team has created a schematic for the board that will be used on the High Voltage side of the system. We used Diptrace as our computer software tool to design the schematic. This is the schematic that will be used to generate the PCB that will be placed where the High Voltage switching equipment is located.

Generate Schematic for Local Control Cabinet Board: The team also created a schematic for the board that will be used inside of the Local Control Cabinet. Just as with the High Voltage Equipment board, Diptrace was used in its creation. This is the schematic that will be used with the creation of the other PCB for the Local Control Cabinet.

Design High Voltage Equipment PCB: With the schematics for the High Voltage Equipment complete, the team has fully designed the printed circuit board. Although the board hasn't yet been physically fabricated, the design has been reviewed and cleared for manufacturing. The VHDL can be loaded onto the board when it has been made to test for "real life" functionality.

Design VHDL Communication Protocol: In order for the boards to perform their desired functions, much coding had to be done. The communications system was written in VHDL with SerDes (Serializer/Deserializer) as the protocol. This is going to control how the boards "talk" to each other and receive/transmit data.

Fig 1: Local control cabinet and high voltage equipment

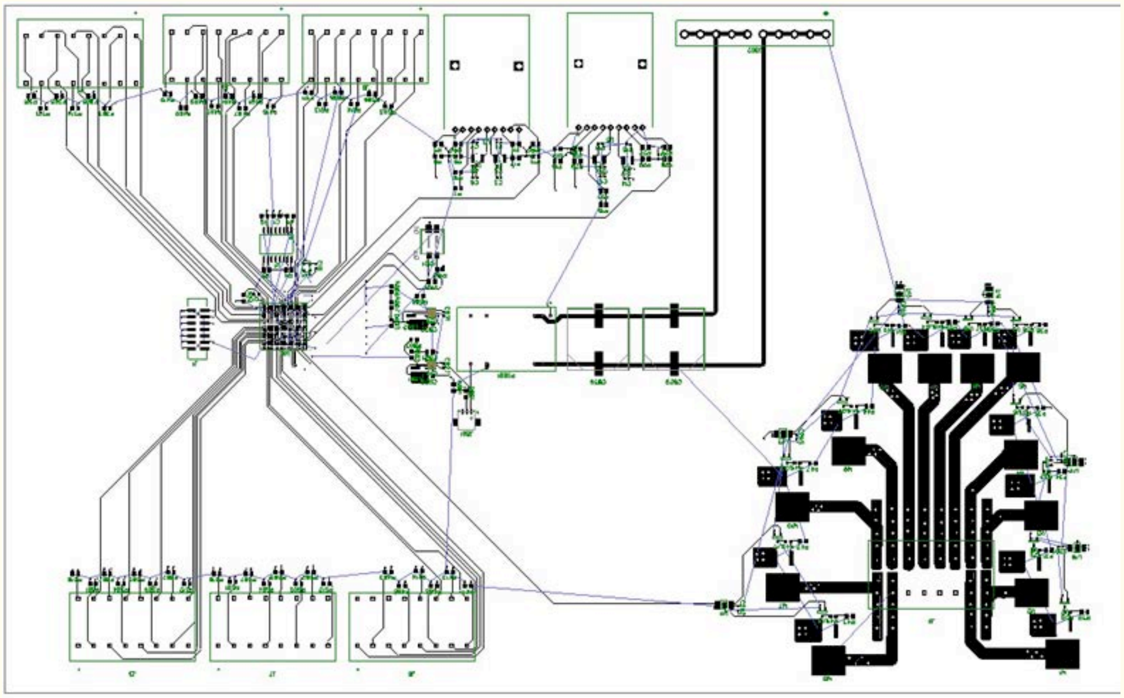

Fig 2: PCB top layer

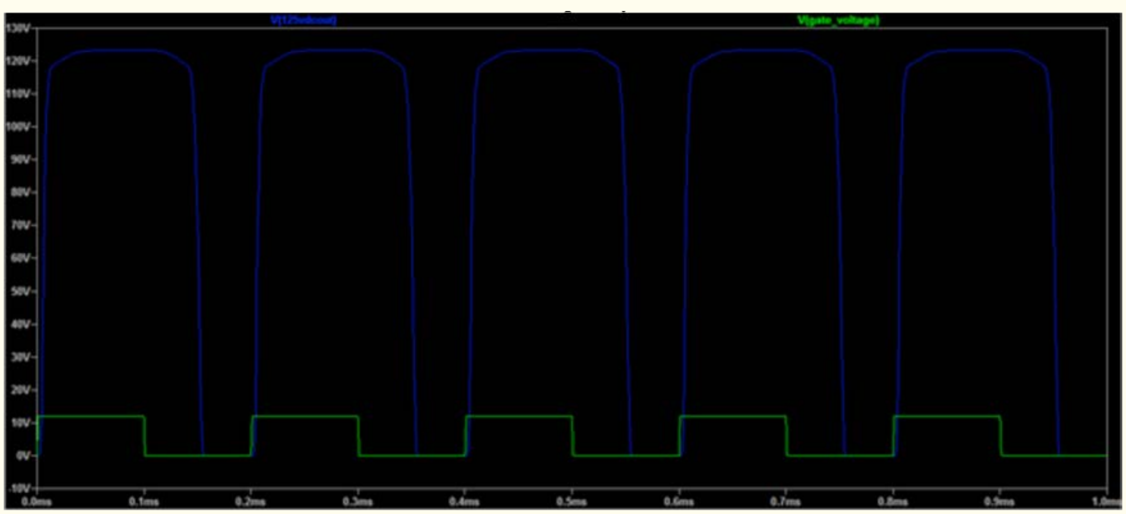

Fig 3: N-Channel MOSFET Gate Voltage and P-Channel MOSFET Gate Voltage vs. Time

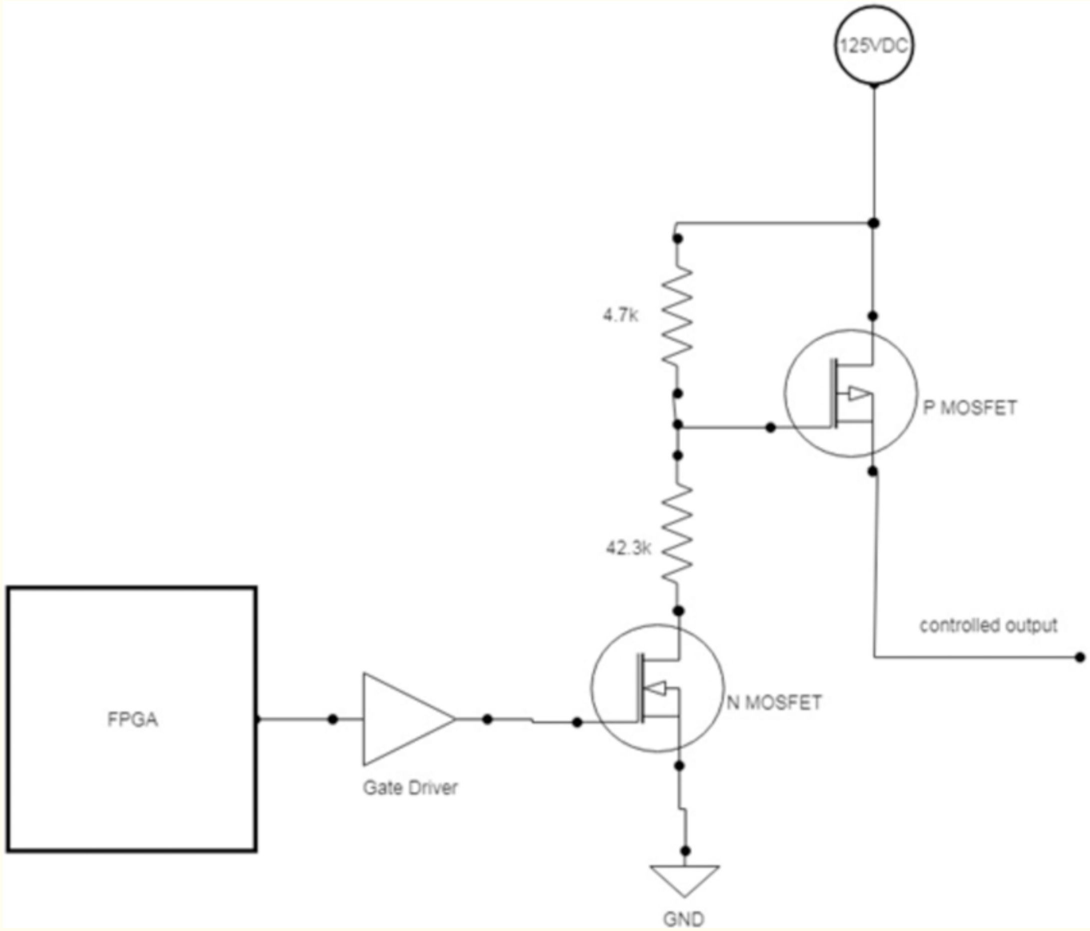

Fig 4: Driving Circuit

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High voltage FPGA

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NET RC<2>  LOC=B2;
NET RC<3>  LOC=A2;
NET RC<4>  LOC=D6;
NET RC<5>  LOC=C6;
NET RC<6>  LOC=B3;
NET RC<7>  LOC=A3;
NET RC<8>  LOC=B4;
NET RC<9>  LOC=A4;
NET RC<10>  LOC=C5;
NET RC<11>  LOC=A5;
NET RC<12>  LOC=B6;

NET SSS1<1>  LOC=G9;
NET SSS2<2>  LOC=F9;
NET SSS3<3>  LOC=B11;
NET SSS4<4>  LOC=A11;
NET SSS5<5>  LOC=B12;
NET SSS6<6>  LOC=A12;
NET SSS7<7>  LOC=B14;
NET SSS8<8>  LOC=A14;
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NET SSS6Return<14>  LOC=C14;
NET SSS7Return<15>  LOC=B16;
NET SSS8Return<16>  LOC=A16;
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Fig 5: User Constraints File Sample for High Voltage Card