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THE UNIVERSITY OF RHODE ISLAND

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# Bench Automation Design for Estimation of Transient Thermal Resistance

ON Semiconductor®

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## Project Motivation

Currently the test for measuring transient thermal resistance is an arduous process. The engineers at ON semiconductor conducting the tests have to set up the equipment manually and record the results from an oscilloscope by eye. After this test the device must cool down before the next test can occur. Oftentimes, the engineer will step away to conduct other work during this cooldown period. This process is time consuming and inefficient. The ultimate design of this project is to have one initial setup for a particular device in order to conduct all of the tests and data collection automatically and efficiently. This includes the system accounting for the cool down requirements before conducting consecutive tests. This will allow the engineers to work as efficiently as possible saving the company countless amounts of man hours in the long run. As the old adage goes “time is money”.

## Key Accomplishments

- **Initial Schematic Design:** Combined two circuit topologies into a single circuit. These circuits are used to measure either SMART or Discrete FETS. This will allow for both testing designs to be implemented on the same PCB. Jacks were added into the schematic to allow for this modularity to be achieved.
- **Push-Pull Design:** In order to choose which resistance is to be used during which test a push-pull design between a PMOS and NMOS was used. These transistors are controlled through a PIC microcontroller which receives a signal from a DLP controller which receives commands from the computer program. This design is shown in **Fig. 3**
- **I/O Reduction:** Reduced the number of input and output needed. Made the push/pull switch topology in the two measuring circuits common. This reduction in input and output needed simplifies the code that the computer engineer needs to create. It will simplify the debugging process in the event that there is a problem with the program.
- **PCB Layout of the Motherboard:** From the combined circuit topology created in OrCAD the combined layout for the motherboard consists of components which allows for a range of tests to be performed.
- **PCB Design Files:** PCB design files were produced for manufacturing purposes.
- **Soldering the motherboard:** The printed circuit board is completed and the components have been soldered to this board. The banana jacks are color coded to simplify the setup process for the engineers conducting the tests. The populated motherboard is shown in **Fig. 2**.
- **Various Bench Equipment Communication:** Communication with Power Supplies, Multimeter, and Oscilloscope have been achieved using Visual Basic, and GPIB communication. We were able to control the output voltage of the Power Supplies, and measure the DC voltage and current from the Multimeter through Graphical User Interface written in Visual Basic. The communication with the Oscilloscope has been accomplished using a USBTMC communication as it didn’t support GPIB for sending commands. We were able to get specific data points from the waveform, and log it in Microsoft Excel. Refer to **Fig. 1**.
- **Device Testing:** Initial testing indicates that the motherboard and daughter card function properly together. The motherboard successfully automates the testing process and we are able to control the level of resistance used for desired power pulses via microcontroller. The PC is able to communicate with microcontroller via SPI frame, and successfully records data from the oscilloscope.
- **Designing the PCB layouts for daughter cards:** Daughter cards for devices under test have been designed and produced. The daughter card we have designed so far is designed according to JEDEC (Joint Electron Device Engineering Council) standards. This design is shown in.
- **Graphical User Interface Design:** The initial user interface program design was improved by adding the flexibility of testing the bench equipments and also the communication with microcontrollers. Hence, it’s ready for final real-test environment. The code for GUI has been cleaned, and organized for future development of the program.
- **Communication with Microcontrollers:** Programmed the DLP microcontroller to send command data to the PIC microcontroller.
- **Debugging:** Initial testing proved unsuccessful, troubleshooting found the issue. Various nmos devices in the push/pull switching topology were incorrect in the PADS library. Issue was rectified with PCB modification. Parts of the board were cut, and new connections were soldered to desired pins.
- **Integrate with the program:** Once the board is tested and determined to be accurate the final step will be to ensure that the automation process is successful by running the range of tests using the computer program to control the various bench equipment and change between which resistance is used.
- **Automated Test:** A successful test was run with the values within the range of acceptable error. The design allowed for the smooth transition between resistor banks. The values found for the device’s transient thermal resistance were as expected.

## Anticipated Best Outcome

A printed circuit board will allow for the testing of various components by merely switching out daughter cards from the main motherboard. This motherboard will include both the discrete and smartFET topologies. The thermal resistance will be measured over the course of twelve tests connected to various resistances. The engineer should be able to set the test conditions in the GUI and allow the data to be collected throughout the day. This data will be populated in an excel spreadsheet for later review by the engineer. This should design should allow for the estimation of thermal resistance on a device by device basis.

## Project Outcome

The Anticipated Best Outcome was achieved. The results from the automated test proves the capability of an automated system for measuring the transient thermal resistance of a smartFET.

## Figures

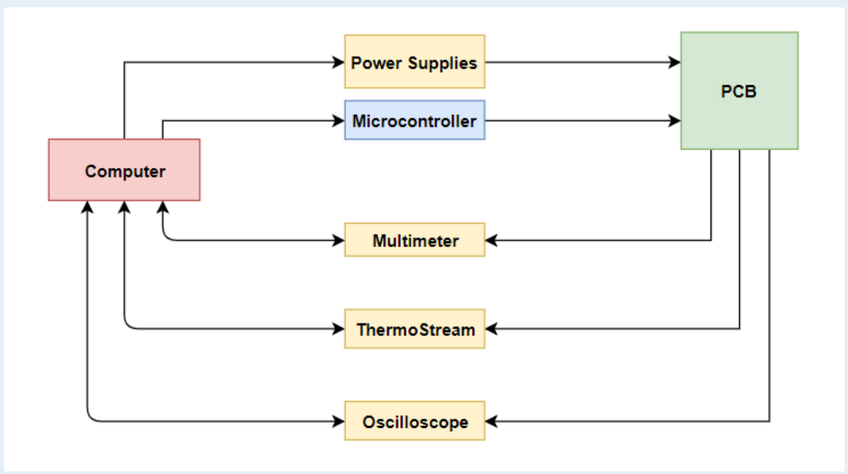


**Fig. 1** System Level Block Diagram

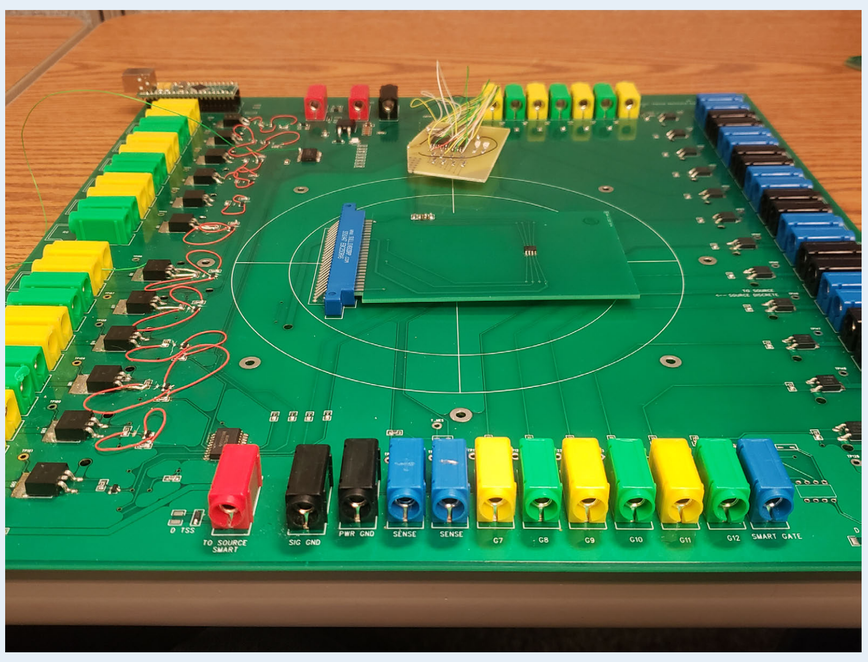

**Fig. 2** Populated Motherboard

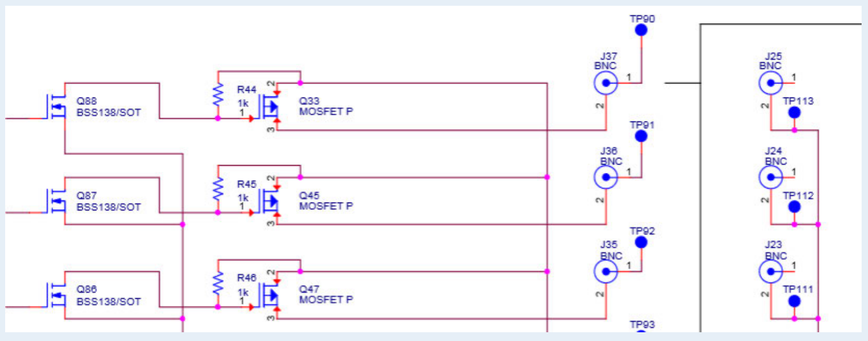


**Fig. 3** Push-Pull Topology

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