ELECOMP CAPSTONE SUMMIT
FRIDAY, MAY 10, 2019

THE UNIVERSITY OF RHODE ISLAND

THINK BIG WE DO℠

Digital Reference Hydrophone for Acoustic System Test

Raytheon

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Project Motivation

Hydrophones are underwater receivers akin to audio microphones. Reference hydrophones are calibrated hydrophones used in support of underwater acoustic systems, such as sonar and acoustic communications systems. The purpose of this Capstone project is to integrate the data acquisition and control functions of a multi-channel test facility into a single-channel capability, transforming the analog reference hydrophone to a digital one. The electronics (with embedded software) will be contained in a small enclosure which provides the interface to an analog hydrophone, provides programmable gain and filtering, analog-digital conversion, two-way synchronization with the transmitting system under test, and an Ethernet interface for control and data. Software on a PC will be required to control the electronics and collect the received data.

Key Accomplishments

General Block Diagram - A block diagram was crucial to understand the full scope of the project and was also used to create a schedule. As a result a diagram of the complete unit including interfaces to subsystems was built.

State Diagrams - Used to structure programs and designs, visualizing the operations of each component. It's very helpful in determining whether changes need to be made to function to spec. On the software side, we used them to sketch and plan the interaction of methods and classes in order to do things like run the main loop on the Java side. For example, we would decide when the main loop would send a packet to check the status of the hardware.

A First Stage Bootloader for Board Writes and for Running - Two separate FSBLs are required in the current version of the Xilinx SDK, one to program the design directly into the board's onboard NOR flash memory, and the other to load the design from that memory after a power cycle.

Functional System in Vivado - To begin implementation of our design on to the board all of the clocks and BRAMs must first be configured in Vivado. A preliminary design was completed that brought out all the necessary ports to finish the FSBL. The handoff file was created and is now ready to be used in the SDK.

Stage 1 & 2 Analog Front End - The first stage of the AFE is composed of an active bandpass filter. This stage has three requirements: impedance matching, filter the incoming signal and supplying gain. The goal is to equalize the input signals of all the 4 hydrophones so that they have similar signal voltages going into the second stage of the AFE. The second stage is composed of 3 lowpass filter and one amplifier circuit that provides additional gain to the signal. This stage has two requirements: filter the incoming signal and supplying gain. The resulting electronic noise from these stages must fall below the required system noise floor.

Schematic Capture-The schematic captured contains the connection of the analog components and the connections from the hardware to the FPGA. It lays out the path from the hydrophone as an analog input signal through the active filters to the ADC. The schematic also contains the connections between the ADC and the FPGA, as well as the path from the FPGA to the Analog components . This path is used as a Test-tone to test the hardware. It also contains the schematic for the power supply of the FPGA MicroZed and analog components.

Completed Programmable Logic - VHDL Modules were written and simulated in Vivado to service each portion of our project. The functions of the VHDL code include: an ADC Interface, ability to externally trigger, accept a trigger, create a test tone, read the parameters from a BRAM, and place all of the samples into BRAM. The hardware has the ability to communicate effectively with the software to monitor the status of the finite state machines. The simulation was performed by creating testbenches that were able to simulate the logic that was implemented.

Full User Datagram Protocol Server and Client - Built in C on the embedded side, and Java on the PC side. The two programs are capable of sending commands to the embedded system from the PC, and sending acoustic data to the PC from the embedded system. The server side on the embedded system is also capable of taking the PC commands and manipulating the board to perform certain functions based on those commands. In addition, the PC client spins off a separate program written in C to transcribe the acoustic data sent from the embedded system into a text file.

Anticipated Best Outcome

The Anticipated Best Outcome was not achieved. The best outcome of this project would be a working hardware interface to a selected reference hydrophone with programmable gain, filtering, test tone, adjustable sample rate, and external trigger. The computer would provide the command and control functions to adjust the hardware settings and capture the data from the digital hydrophone, while displaying the time series and FFT. The analog interface was designed and simulated. The firmware and software were completed.

Project Outcome

The Anticipated Best Outcome was not achieved. However, all of the software and firmware were completed as outlined at the beginning of the year. Schematic Capture for the board was completed, but not layout, fabrication, or assembly. As of now an internal test tone loop can verify that the firmware and hardware function correctly.

Figures

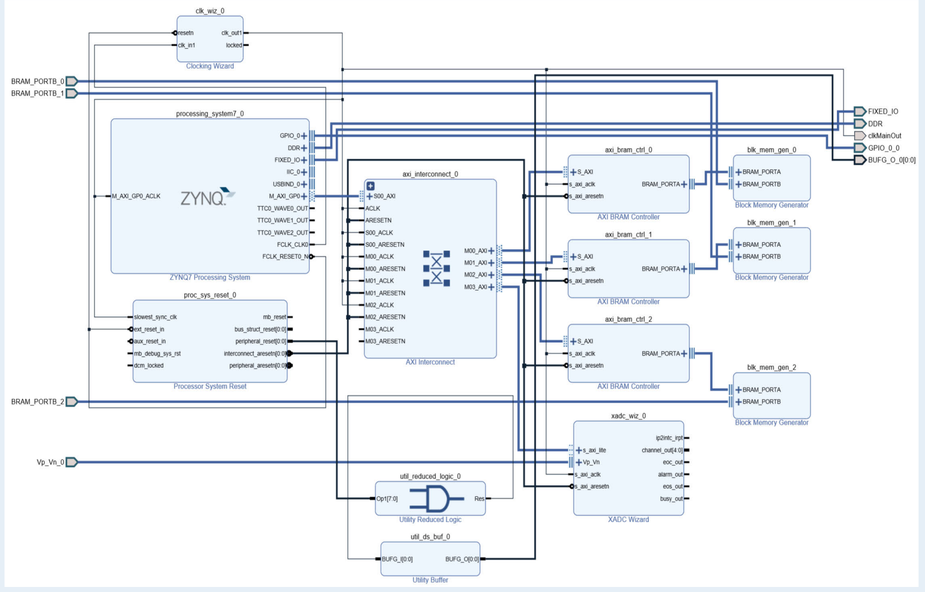

Fig. 1: Block Diagram of Programmable System in Vivado

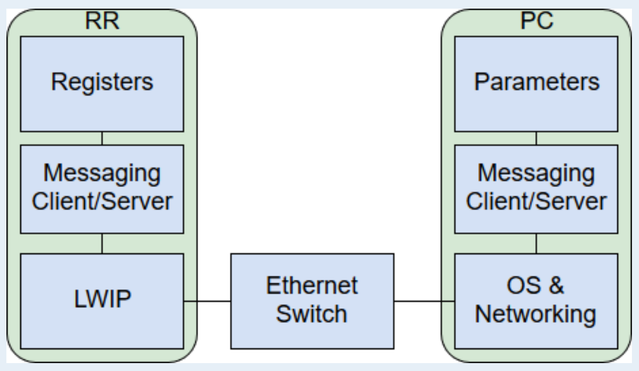

Fig. 2: Block Diagram of software interface between FPGA and PC

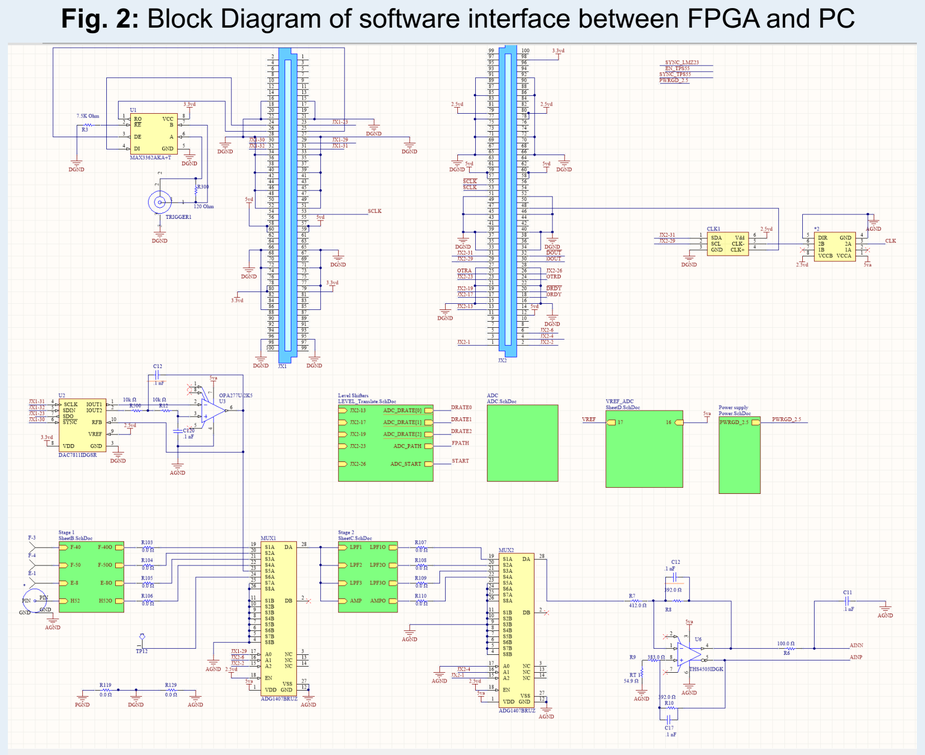

Fig. 3: Schematic Capture of the Analog Front End

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